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CP306-V

3U CompactPCI
Celeron® M / Pentium® M Based
CPU Board

Manual ID: 28545, Rev. Index 01
November 2004

USER GUIDE

28545.01.UG.VC.041104/162917

The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CP306-V	
Manual ID Number:	28545	
Rev. Index	**Brief Description of Changes**	**Date of Issue**
01	User Guide	Nov 2004

Imprint

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Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.

Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

- In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Two Year Warranty

Kontron Modular Computers GmbH grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron Modular Computers GmbH.

Kontron Modular Computers GmbH warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron Modular Computers GmbH or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron Modular Computers GmbH, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the home page of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to Kontron Modular Computers CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine Kontron’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of Kontron CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing Kontron CompactPCI boards with links to the relating data sheets.
- Generic information on the Kontron CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the Kontron CompactPCI standard backplane family.
- Generic information on the Kontron CompactPCI power supply units, such as the input/ output characteristics, redundant operation and distinctive features, as well as an overview of the Kontron CompactPCI standard power supply unit family.

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1.2 Board Overview

1.2.1 Board Introduction

The CP306-V is a CompactPCI system controller board. It has been designed to support all Intel® Celeron® M and Pentium® M processors with 400 MHz PSB (Processor Side Bus) in 478 µFCPGA packaging.

A key performance factor of the Intel Celeron M and Pentium M processors is the newly designed CPU core with an integrated 64 kB L1 and up to 2048 kB L2 cache, which provide more CPU power per MHz than an Intel Celeron® or an Intel Pentium® 4 processor.

The Celeron M and Pentium M have the advantage of very low power consumption, whilst at the same time providing impressive processor speeds ranging from 600 MHz through 2.0 GHz with a Processor Side Bus (PSB) running at 400 MHz. The CP306-V utilizes the Intel 855GME and I/O Controller Hub 4 (ICH4) chipset.

The board includes a SODIMM socket for up to 1 GB Double Data Rate (DDR) memory with Error Checking and Correcting (ECC) for rugged environments. The memory operates at 333 MHz (PC2700).

The CP306-V offers more features and expandability than other CompactPCI boards in its class. The board comes with two onboard Ultra ATA/100 interfaces and a built-in Intel 3D Graphics accelerator with up to 64 MB of shared memory for enhanced graphics performance with a DVI display interface on the front panel. Furthermore, the front panel provides one Fast Ethernet port (integrated in the chipset), one USB 2.0 port, one COM port (8HP only) and one PS/2 connector for mouse and keyboard. Several onboard connectors provide flexible expandability.

The board supports one configurable 32-bit/33 MHz CompactPCI interface.

The optional extension module provides a CompactFlash type II socket on the front panel. On this module it is possible to mount a 2.5” hard disk drive using a 44-pin connector.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments, including I/O intensive applications, making it a perfect core technology for long life applications. Components which have high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability.

The board is offered with the Microsoft® Windows® 2000, Windows® XP operating systems. Kontron further supports, as a standard, Windows® XP Embedded, Linux and VxWorks operating systems. Please contact Kontron Modular Computers for further information concerning other operating systems.

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1.2.2 Board-Specific Information

The CP306-V is a CompactPCI Celeron M and Pentium M based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP306-V's outstanding features are:

- Socket for Intel Celeron M and Pentium M microprocessors up to 2.0 GHz (and higher when available) in a 478 µFCPGA package
- Up to 2048 kB L2 cache on-die, running at CPU speed
- 400 MHz processor system bus
- 855GME and 82801DB (ICH4) chipset
- SODIMM socket for up to 1024 MB DDR SDRAM memory running at 333 MHz (PC2700)
- Integrated 3D high performance VGA controller
- Digital (DVI) display support with up to 1600x1200 pixels at 24-bit and 60 Hz
- Analog display support with up to 2048 x 1536 pixels at 16-bit and 60 Hz
- One Fast Ethernet interface (82559-style)
- Two EIDE Ultra ATA/100 interfaces
- One front USB 2.0 port
- Two rear I/O USB 2.0 ports
- Compatible with CompactPCI spec. Rev. 3.0
- 1 MB onboard FWH for BIOS
- Hardware Monitor (LM87)
- Watchdog timer
- Real-time clock
- Two COM ports
  - One switchable to front or rear I/O
  - One only for rear I/O
- I/O extension connector (LPC)
- 8HP or 4HP, 3U CompactPCI
- Several rear I/O configurations
- Jumperless board configuration
- Standard temperature range: 0°C to + 60°C
- Passive heat sink solution
- Phoenix BIOS

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1.3 Optional Modules

1.3.1 CP306-V-IOIDE Module

The CP306-V-IOIDE module has been designed to provide the CP306-V with a CompactFlash socket and an interface to a 2.5” HDD which enable the user to connect P-ATA devices to the board. Furthermore, the module provides a Reset button and an LED indicating the operation of EIDE devices. The module is connected to the 44-pin EIDE Connector J11 on the 8HP version of the CP306-V. Refer to Appendix A for further information on the CP306-V-IOIDE module.

1.3.2 CP-RIO3-03 Rear I/O Module

Designed for use with a 32-bit rear I/O variant of the CP306-V and a backplane with system slot rear I/O capability, this module provides rear I/O interfacing for the two standard RS232 serial interfaces, one Fast Ethernet interface, two USB 2.0 interfaces, one primary EIDE interface, one PS/2 interface, one fan sense signal. Refer to Appendix B for further information on the CP-RIO3-03 Rear I/O module.

1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP306-V.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
System Configuration	A CP306-V master board can support up to 7 peripheral boards with 32-bit and 33 MHz.
Master/Slave Functionality	The CP306-V can operate only as a master board.
Board Location in the System	The CP306-V board must be installed in a master slot of a CompactPCI backplane.
Hot Swap Compatibility	The CP306-V supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and ENUM signal handling are in compliance with the PICMG 2.1 Hot Swap specification.The CP306-V itself is not hot swap capable.
Hardware Requirements	The CP306-V can be installed in any CompactPCI 3U rack.
Operating Systems	The CP306-V can operate under the following operating systems: Microsoft Windows 2000 Microsoft Windows XP Microsoft Windows XP Embedded Linux VxWorks Please contact Kontron Modular Computers for further information concerning other operating systems.

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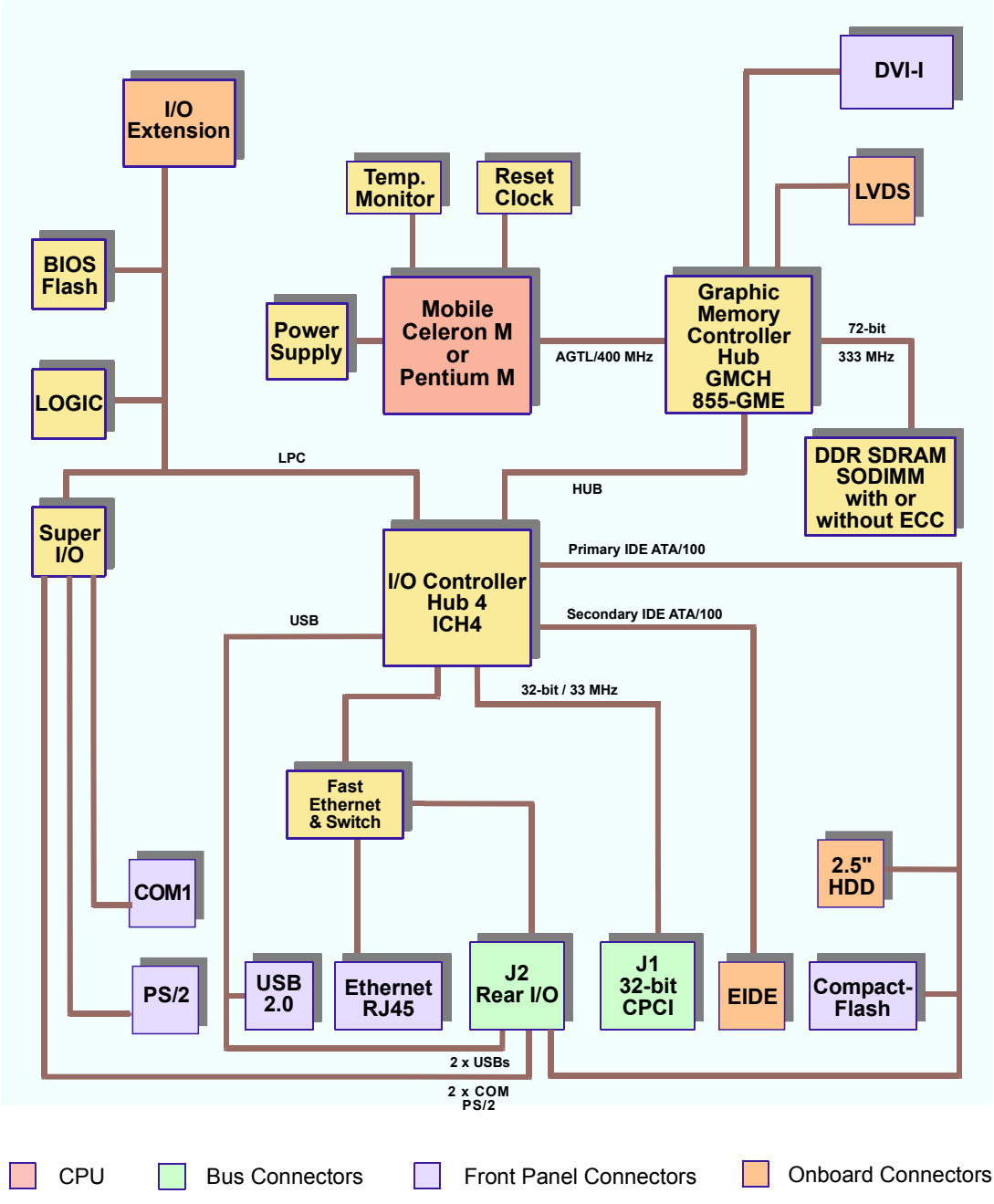
1.5 Board Diagrams

The following diagram provides additional information concerning board functionality and component layout.

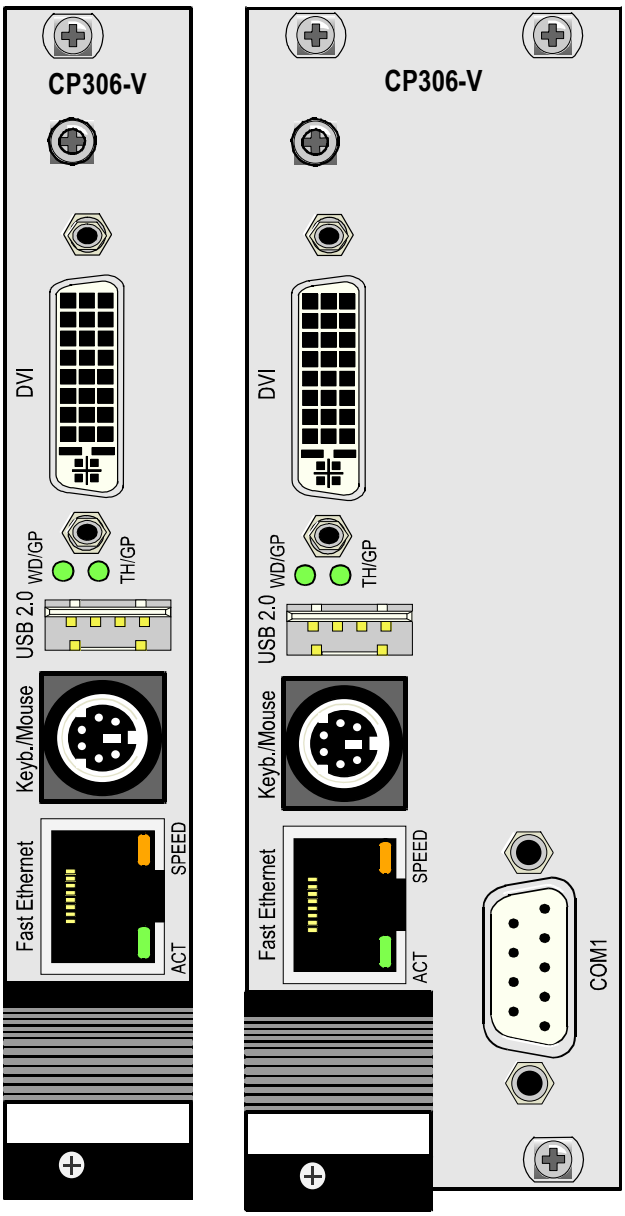
1.5.1 Functional Block Diagram

Figure 1-1: CP306-V Functional Block Diagram



1.5.2 Front Panels

Figure 1-2: 4HP and 8HP Front Panel of CP306-V without Module



4 HP 8 HP

LEGEND:

CP306-V: 4HP and 8HP version

General Purpose LEDs

- WD/GP (green): Watchdog or General Purpose; when lit during bootup, it indicates a PCI reset is active.
- TH/GP (green): Overtemperature Status or General Purpose; when lit during bootup, it indicates a power failure.

Integral Ethernet LEDs

- ACT (green): Ethernet Link/Activity
- SPEED (orange): Ethernet Speed

Fast Ethernet

- Speed on: 100 Mbit
- Speed off: 10 Mbit

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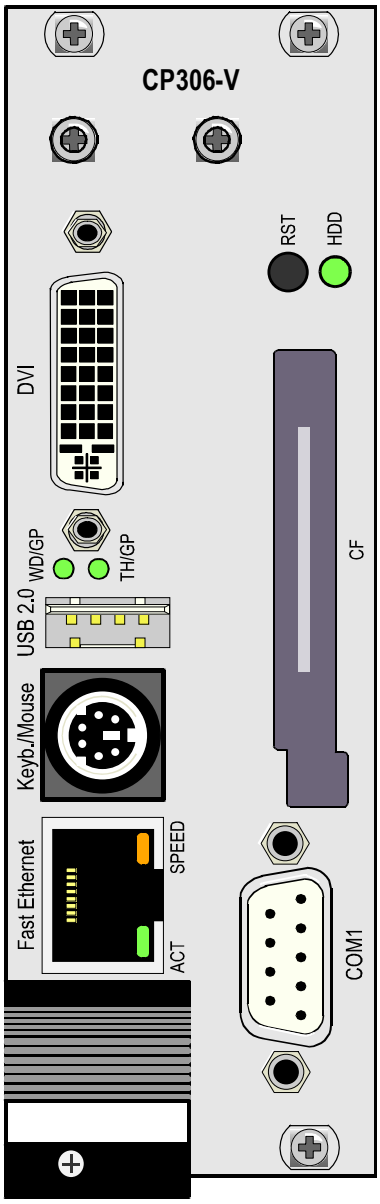
Figure 1-3: 8HP Front Panel of CP306-V with CP306-V-IOIDE Module



LEGEND:

CP306-V: 8HP version

General Purpose LEDs

- WD/GP (green): Watchdog or General Purpose; when lit during bootup, it indicates a PCI reset is active.
- TH/GP (green): Overtemperature Status or General Purpose; when lit during bootup, it indicates a power failure.
- HDD (green): Monitors hard disk activity

Reset Button

- RST: Reset button

Integral Ethernet LEDs

- ACT (green): Ethernet Link/Activity
- SPEED (orange): Ethernet Speed

Fast Ethernet

- Speed on: 100 Mbit
- Speed off: 10 Mbit

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1.5.3 Board Layouts

Figure 1-4: CP306-V Board Layout (Top View)

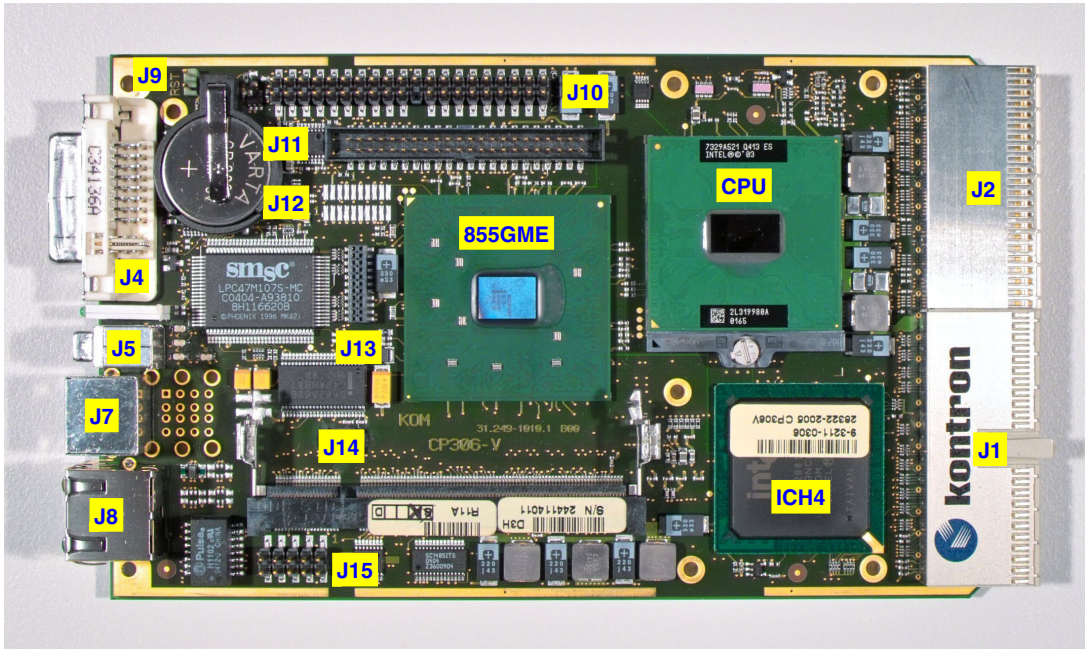
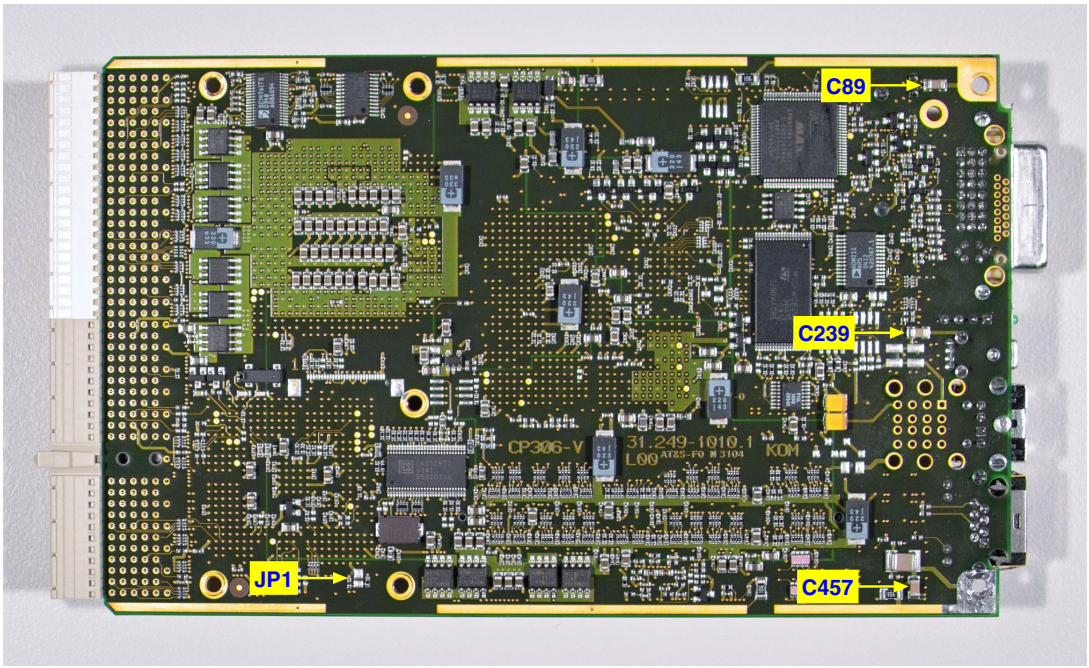


Figure 1-5: CP306-V Board Layout (Bottom View)



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1.6 Technical Specification

Table 1-2: CP306-V Main Specifications

	CP306-V	SPECIFICATIONS

Processor and Memory	CPU	The CP306-V supports the following microprocessors:
		• Intel Celeron M processors with 400 MHz PSB (Processor Side Bus) in 478 µFCPGA packaging
		  • Intel Celeron M 1.3 GHz with 512 kB L2 cache
		• Intel Pentium M processors with 400 MHz PSB (Processor Side Bus) and SpeedStep® technology in 478 µFCPGA packaging
		  • Intel Pentium M 1.6 GHz with 1 MB L2 cache
		  • Intel Pentium M 745, 1.8 GHz with 2 MB L2 cache
		Please contact Kontron Modular Computers for further information concerning the suitability of other Intel processors for use with the CP306-V.

	Memory	Main Memory:
		• Up to 1024 MB DDR333 (PC2700) DDR SDRAM memory on SODIMM module
		Cache structure:
		• 64 kB L1 on-die full speed processor cache
		  • 32 kB for instruction cache
		  • 32 kB for data cache
		• Up to 2048 kB L2 on-die full speed processor cache
		FLASH Memory:
		• 1 MB FLASH for BIOS
		Mass Storage Device (only with CP306-V-IOIDE extension module):
		• CompactFlash socket type II (true IDE mode with DMA support)
		Serial EEPROM: 24LC64 (64 kbit)

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Table 1-2: CP306-V Main Specifications (Continued)

	CP306-V	SPECIFICATIONS
Chipset	Intel 855GME chipset	855GME Graphics Memory Controller Hub (GMCH) • Support for a single Celeron M or Pentium M microprocessor • 64-bit AGTL/AGTL+ based System Bus interface at 400 MHz • 64-bit System Memory interface with optimized support for DDR SDRAM memory at 333 MHz with ECC (additional 8-bits for ECC) • Integrated 2D and 3D Graphics Engines • Integrated H/W Motion Compensation Engine • Integrated 350 MHz DAC
	Intel ICH4	82801DB I/O Controller Hub (ICH4) • PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations • Power management logic support • Enhanced DMA controller, interrupt controller, and timer functions • Integrated IDE controller Ultra ATA/100/66/33 • USB 2.0 host interface six USB ports • One integrated LAN controller (82559 style) • System Management Bus (SMBus) compatible with most I²C™ devices • Low Pin Count (LPC) interface • Firmware Hub (FWH) interface support
Interfaces	CompactPCI	Compliant with CompactPCI Specification PICMG® 2.0 R 3.0 • System master operation • 32-bit / 33 MHz master interface • 3.3V / 5.0V compatible (default configuration is 5.0V)
	Rear I/O	The following interfaces are routed to the rear I/O connector J2: • COM1 and COM2 (TTL signaling) • 2 x USB 2.0 • 2x fan sense • CRT VGA • Fast Ethernet • Primary EIDE • General purpose signals • PS/2 mouse and keyboard
	Hot Swap	The CP306-V supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and Enum signal handling are in compliance with the PICMG 2.1 Hot Swap Specification. The CP306-V itself is not hot swap capable.
	VGA	Built-in Intel 3D Graphics accelerator for enhanced graphics performance. • Supports resolutions of up to 2048 x 1536 by 16-bit at a 60 Hz refresh rate or up to 1280 x 1024 by 24-bit true colors at 85 Hz refresh rate in analog mode (CRT). • Hardware motion compensation for software MPEG2 and MPEG4 de-coding • The graphics controller provides flexible allocation of video memory up to 64 MB.

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Table 1-2: CP306-V Main Specifications (Continued)

	CP306-V	SPECIFICATIONS
Interfaces	Fast Ethernet	One 10Base-T/100Base-TX Fast Ethernet port integrated within the ICH4 controller (82559-style): • One RJ45 connector on the front panel • Support for rear I/O interfacing • May only be operated at either of the above interfacing points • Automatic mode recognition Cabling requirement: Category 5, UTP, two-pair cabling.
	USB	Up to three USB ports supporting UHCI and EHCI: • One USB 2.0 connector on the front panel • Two USB 2.0 connectors on the rear I/O interface
	Serial	Two UARTs, 16C550 compatible. • Two for rear I/O, whereas one of them can be switched over to front panel
	Keyboard and Mouse	Keyboard and mouse are supported • USB Support on 8HP and 4HP • PS/2 on front panel or rear I/O

	Mass Storage	EIDE Ultra ATA/100/66/33
		• Two interfaces
		  • Primary interface routed to rear I/O and a 44-pin, 2 mm, male pin-row connector, for example, for mounting the CP306-V-EXT-IO-IDE module or a 2.5” HDD
		  • Secondary interface routed to a 40-pin, 2.54 mm, male pinrow connector (standard)
		• Up to four EIDE devices
		CompactFlash (with extension module only):
		• CompactFlash type II socket (true IDE mode with DMA support)
		• Supports type I and II CompactFlash cards and Microdrive

	I/O Extension Interface	I/O extension interface: • Female, pinrow connector • LPC devices

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Table 1-2: CP306-V Main Specifications (Continued)

	CP306-V	SPECIFICATIONS
General	Mechanical	3U CompactPCI compliant form factor 4HP and 8HP versions
	Power Consumption	See Chapter 6 for details
	Temperature Range	Operational: 0°C to +60°C Standard Storage: -55°C to +85°C Without hard disk -40°C to +65°C With hard disk
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 160 mm
	Board Weight	4HP: 334 grams (with heat sink) 8HP: 410 grams (with heat sink and without mezzanine boards)
	Battery	3.0V lithium battery for RTC with battery socket. Recommended types: • VARTA CR2025 • PANASONIC BR2020
Sockets	Front Panel Connectors	• DVI-I: 29-pin connector for DVI or CRT devices • USB: one 4-pin USB connector • Ethernet: one RJ-45 connector • PS/2: one 6-pin connector for mouse and keyboard • CompactFlash: one 50-pin connector, optional • RS232: one D-SUB 9 connector
	Onboard Connectors	• Two EIDE interfaces supporting Ultra ATA/100/66/33 for two devices (hard disks or CD-ROMs) on 40-pin/2.54mm and 44-pin/2 mm connectors. • I/O extension connector • CompactPCI Connector J1 and J2 • 478 µFCPGA socket for Celeron M and Pentium M CPUs • 200-pin socket for DDR SODIMM modules with or without ECC

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Table 1-2: CP306-V Main Specifications (Continued)

	CP306-V	SPECIFICATIONS
HW Monitoring	LEDs	System status: • TH/GP: green: Overtemperature status or general purpose; when remains lit during bootup, it indicates a power failure. • WD/GP: green: Watchdog or general purpose; when remains lit during bootup, it indicates a PCI reset is active Fast Ethernet status: • ACT: green: Network activity • SPEED on: orange: 100 Mbit • SPEED off: 10 Mbit
	Watchdog	Software configurable Watchdog generates IRQ, NMI, or hardware reset.
	Thermal Management	CPU overtemperature protection is provided by: • Internal processor temperature control unit • CPU shut down via hardware monitor • Custom designed heat sinks
	System Monitor	LM87 hardware monitor for supervision of: • All system power voltages • Two fan speed inputs
Software	Software BIOS	Phoenix BIOS with 1 MB of Flash memory and having the following features: • QuickBoot • QuietBoot • MultiBoot III • LAN-boot capability for diskless systems • Boot from USB floppy • BIOS boot support for USB keyboards • Software enable/disable function for the rear I/O, Ethernet • Plug and play capability • BIOS parameters are saved in the EEPROM • Board serial number is saved within the EEPROM • PC Health Monitoring
	Operating Systems	Operating systems supported: • Microsoft Windows 2000 • Microsoft Windows XP • Microsoft Windows XP Embedded • Linux • VxWorks Please contact Kontron Modular Computers for further information concerning other operating systems.

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1.7 Kontron Software Support

Kontron is one of the few CompactPCI and VME vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with *Kontron* can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

1.8 Applied Standards

The *Kontron Modular Computers'* CompactPCI systems comply with the requirements of the following standards.

Table 1-3: Applied Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL (RUGGEDIZED VERSION)
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental Aspects	Vibration (Sinusoidal)	IEC60068-2-6	5g/10-300Hz/10 acceleration / frequency range / 10 cycles per axis
	Random Vibration (Broadband)	IEC 60068-2-64 (3U boards)	20-500Hz,0.05g²/500-2000Hz, 0.005g²/3.5g rms/30min./axis frequency range1 / frequency range2 / acceleration / cycle / duration
	Permanent Shock	IEC60068-2-29	15g/11ms/500/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC60068-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in sec.
	Climatic Humidity	IEC 60068-2-78	93% RH at 40°C, non-condensing

Note ...

The values in the above table are valid for boards which are ordered with the ruggedized service. For more information, please contact your local Kontron office.

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1.9 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 2.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	Hot Swap Specification PICMG 2.1
	PEP Modular Computers' CompactPCI System Manual, ID 19954
CompactFlash Cards	CF+ and CompactFlash Specification Revision 2.1

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The CP306-V supports the latest Intel Celeron M and Pentium M processor family up to speeds of 2.0 GHz. The Intel Celeron M and Pentium M microprocessors offer exceptional performance with low power consumption. These processors are based on a new core which is optimized for low power consumption.

The Intel Pentium M supports the latest Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. The frequency for the Pentium M processor may also be selected in the BIOS.

The following list sets out some of the key features of this processor:

- Supports Intel Architecture with Dynamic Execution
- High performance, low power core
- On-die, primary 32 kB instruction cache and 32 kB write-back data cache
- On-die, second level cache with Advanced Transfer Cache Architecture
  - Intel Celeron M with 512 kB L2 cache
  - Intel Pentium M with 1024 kB L2 cache
  - Intel Pentium M with 2048 kB L2 cache
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400 MHz, source-synchronous processor system bus
- Advanced Power Management features including Enhanced Intel SpeedStep Technology (only Intel Pentium M processors)

The following tables provide information on the Intel Celeron M processor supported on the CP306-V and its maximum power dissipation.

Table 2-1: Supported Intel Celeron M Processor on the CP306-V

SPEED	1.3 GHz
PACKAGE	µFCPGA
L2 CACHE	512 kB
CORE VOLTAGE	1.356 V
PROCESSOR SIDE BUS	400 MHz

Table 2-2: Maximum Power Dissipation of Intel Celeron M (CPU only)

FREQUENCY MODE	1.3 GHz
Maximum Power	24.5 W

Note ...

The Intel Celeron M processor does not support the Intel SpeedStep feature. This processor always runs with a fixed frequency.

The following tables indicate the Intel Pentium M processors supported on the CP306-V, their maximum power dissipation and their core voltage in the various frequency modes.

Table 2-3: Supported Intel Pentium M Processors on the CP306-V

SPEED	1.6 GHz	1.8 GHz	2.0 GHz
PACKAGE	µFCPGA	µFCPGA	µFCPGA
L2 CACHE	1024 kB	2048 kB	2048 kB
CORE VOLTAGE	0.956 - 1.484 V	0.988 - 1.276 V	0.988 - 1.276 V
PROCESSOR SIDE BUS	400 MHz	400 MHz	400 MHz

Table 2-4: Maximum Power Dissipation of Intel Pentium M (CPU only)

FREQUENCY MODE	1.6 GHz	1.8 GHz	2.0 GHz
Maximum Power HFM[1)]	25.4 W	21 W	21 W
Maximum Power LFM[2)]	4 W	7.5 W	7.5 W

[1)]HFM High Frequency Mode (maximum frequency of the CPU)

[2)]LFM Low Frequency Mode (frequency is 600 MHz)

Table 2-5: Intel Pentium M Core Voltage in the Various Frequency Modes

FREQUENCY	Vcore		
	1.6 GHz	1.8 GHz	2.0 GHz
2.0 GHz			1.276 V
1.8 GHz	--	1.276 V	1.244 V
1.6 GHz	1.484 V	1.228 V	1.196 V
1.4 GHz	1.420 V	1.180 V	1.164 V
1.3 GHz	--	--	--
1.2 GHz	1.276 V	1.132 V	1.116 V
1.1 GHz	--	--	--
1.0 GHz	1.164 V	1.084 V	1.084 V
900 MHz	--	--	--
800 MHz	1.036 V	1.036 V	1.036 V
600 MHz	0.956 V	0.988 V	0.988 V

Note ...

Due to the fact that the Pentium M 755 2.0 GHz processor is not on the Intel embedded roadmap, we cannot assure long-term availability of this processor. Therefore, this processor is intended for use only on future customized CP306-V boards.

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2.1.2 Memory

The CP306-V has one 200-pin SODIMM socket J14 for up to 1024 MB DDR333 memory, and it also supports ECC.

Table 2-6: Supported Memory Extension for SODIMM Module

MEMORY WITH ECC	MEMORY WITHOUT ECC	TOTAL SYSTEM MEMORY
256	256	256
512	512	512
1024	1024	1024

Note ...

If memory modules without ECC are used, the memory errors cannot be corrected.

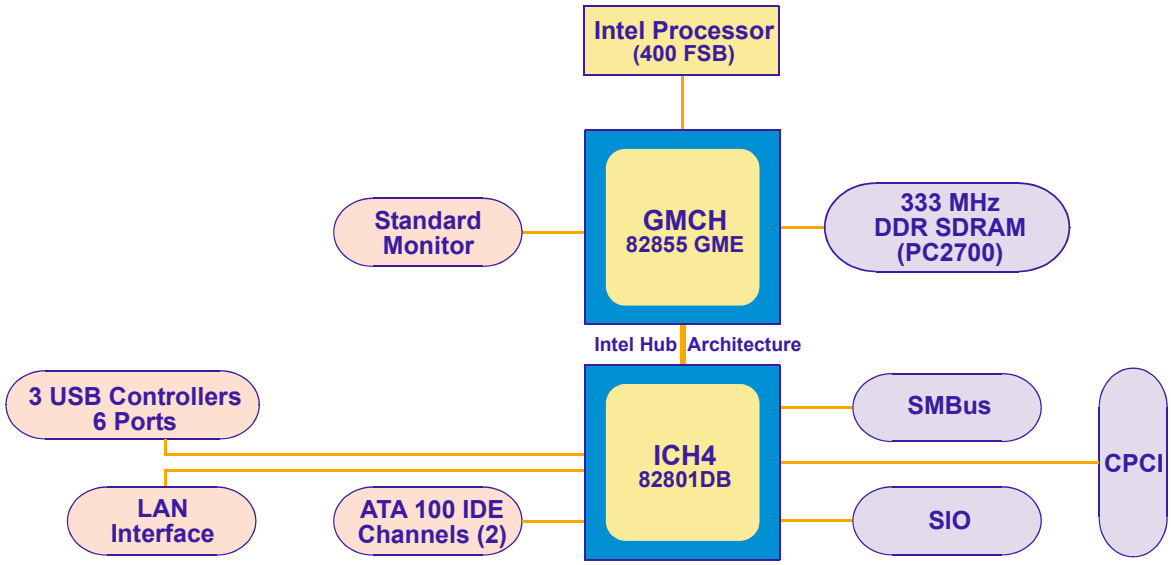
2.1.3 855GME Chipset Overview

The Intel 855GME chipset consists of the following devices:

- 82855GME Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801DB I/O Controller Hub 4 (ICH4) with AHA bus
- M50FW080 Firmware Hub (FWH)

The GMCH provides the processor interface for the Celeron M and Pentium M microprocessors, the memory bus and includes a high performance graphics accelerator. The ICH4 is a centralized controller for the boards' I/O peripherals, such as the CompactPCI, USB 2.0, EIDE, and LAN ports. The Firmware Hub (FWH) provides the non-volatile storage for the BIOS.

Figure 2-1: 855GME Chipset Functional Block Diagram



2.1.4 Graphics and Memory Controller Hub (855GME)

The 855GME Graphics Memory Controller Hub (GMCH) is a highly integrated hub that provides the CPU interface (optimized for the Intel Celeron M and Pentium M), the DDR SDRAM system memory interface (optimized for DDR200/PC1600, DDR266/PC2100 and DDR333/ PC2700), a hub link interface to the ICH4 and high performance internal graphics.

Graphics and Memory Controller Hub Feature Set

Host Interface

The 855GME is optimized for the Intel Celeron M and Pentium M microprocessors. The chipset supports a Processor Side Bus (PSB) frequency of 400 MHz using 1.05 V AGTL signalling. Single-ended AGTL termination is supported for single processor configurations. The AGTL bus supports 32-bit host addressing for decoding up to 4 GB memory address space.

System Memory Interface

The 855GME integrates a system memory Dual Data Rate (DDR) SDRAM controller with a 72-bit wide interface including ECC bits. The chipset supports DDR200, DDR266 and DDR333 (PC1600, PC2100 and PC2700) DDR SDRAM for system memory.

855GME Graphics Controller

The 855GME includes a highly integrated graphics accelerator and H/W Motion Compensation engines for software MPEG2 decoding delivering high performance 3D and 2D video capabilities. The internal graphics controller provides an interface for a standard DVI port that supports digital and analog displays.

2.1.5 I/O Controller Hub ICH4

The ICH4 is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms, for example, Ultra DMA 100/66/33 controller, USB host controller supporting USB 2.0, LPC interface, FWH Flash BIOS interface controller, and LAN interface. The ICH4 communicates with the host controller over a dedicated hub interface.

I/O Controller Hub Feature set comprises:

- PCI 2.2 interface with eight IRQ inputs
- Bus Master EIDE controller UltraDMA 100/66/33
- Three USB controllers with six USB 1.1 or USB 2.0 ports
- Hub interface for a 855GME chipset
- FWH interface
- LPC interface
- Integrated LAN controller, 82559-style
- RTC controller

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2.2 Peripherals

The following standard peripherals are available on the CP306-V board:

2.2.1 Timer

The CP306-V is equipped with the following timers:

- Real-Time Clock
  The ICH4 contains a MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM.
  The real-time clock performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss.
- Counter/Timer
  Three 8254-style counter/timers are included on the CP306-V as defined for the PC/AT.

2.2.2 Watchdog Timer

A watchdog timer is provided, which forces either an IRQ5, NMI, or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped.

2.2.3 Battery

The CP306-V is provided with a 3.0 V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020.

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Warning!

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.

To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

2.2.4 Reset

The CP306-V is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5 V line and below 3.0 V for the 3.3 V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer, an onboard reset jumper on the 4HP version, a reset push button on the 8HP version, and a CompactPCI reset. The CP306-V responds to any of these sources by initializing local peripherals.

A reset will be generated if one of the following events occur:

- +5 V supply falls below 4.725 V
- +3.3 V supply falls below 3.0 V
- Power failure of the DC/DC converter for the processor
- Onboard reset jumper is set (J9)
- Watchdog overflow
- CompactPCI backplane PRST input
- Reset push button is pressed

2.2.5 SMBus Devices

The CP306-V provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I^2C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-7: SMBus Device Addresses

DEVICE	SMB ADDRESS
Hardware Monitor LM87	0101110xb
EEPROM 24LC64	1010111xb
Clock	1101001xb
SPD	1010000xb

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2.2.6 Thermal Management/System Monitoring

The LM87 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures, all of which are very important for the proper operation and stability of a high-end computer system. The LM87 provides an I²C serial bus interface.

The voltages of the onboard power supply core; +12 V, -12 V, +5 V, +3.3 V, +2.5 V, and Vcore are supervised. Two fan tachometer outputs can be measured using the LM87's FAN1 and FAN2 inputs.

The temperature sensors on the LM87 monitor the CPU temperature and the ambient temperature around the CPU to ensure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduce the CPU clock duty cycle, depending on the mode chosen in BIOS.

2.2.7 Serial EEPROM

This EEPROM is connected to the I²C bus provided by the ICH4.

Table 2-8: EEPROM Address Map

ADDRESS	FUNCTION
0x000 - 0x0FF	CMOS backup
0x100 - 0x1FF	Production data
0x200 - 0x3FF	OS Bootparameter
0x400 - 0x7FF	User

2.2.8 BIOS FLASH (Firmware Hub)

For simple BIOS updating a standard onboard 1 MB Firmware Hub device is used.

The FWH stores both the system BIOS and video BIOS. It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the Phoenix Phlash16 utility.

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2.3 Board Interfaces

2.3.1 General Purpose LED Output

The CP306-V provides two software programmable GP LEDs. After reset the default configuration for the two front LEDs is Overtemperature and Watchdog status. Additionally, if the WD LED remains on during bootup, it indicates a PCI reset is active, and if the TH LED remains on during bootup, it indicates a power failure. In this case, please check the power supply. If the power supply appears to be functional and this LED remains on, please contact Kontron Support. The LEDs can be configured via two onboard registers. For more information please see Chapter 4 Configuration.

The LED control logic remains in the same state until the next system reset.

Note ...

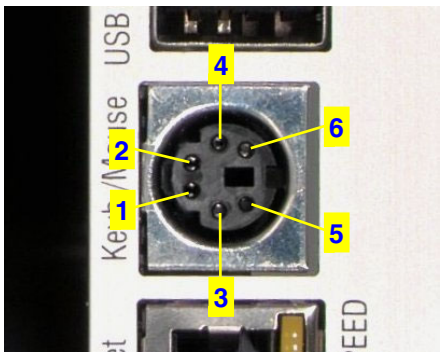
If the overtemperature LED flashes on and off at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature.

Once activated, Thermtrip remains latched until a cold restart of the CP306-V is undertaken (all power off and then on again).

2.3.2 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

Figure 2-2: Keyboard/Mouse Connector J7



The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded Mini-DIN connector. The keyboard power supply unit provides 500 mA continuous load current and a short-circuit protection (900 mA). All signal lines are EMI filtered.

Table 2-9: Keyboard Connector J7 Pinout

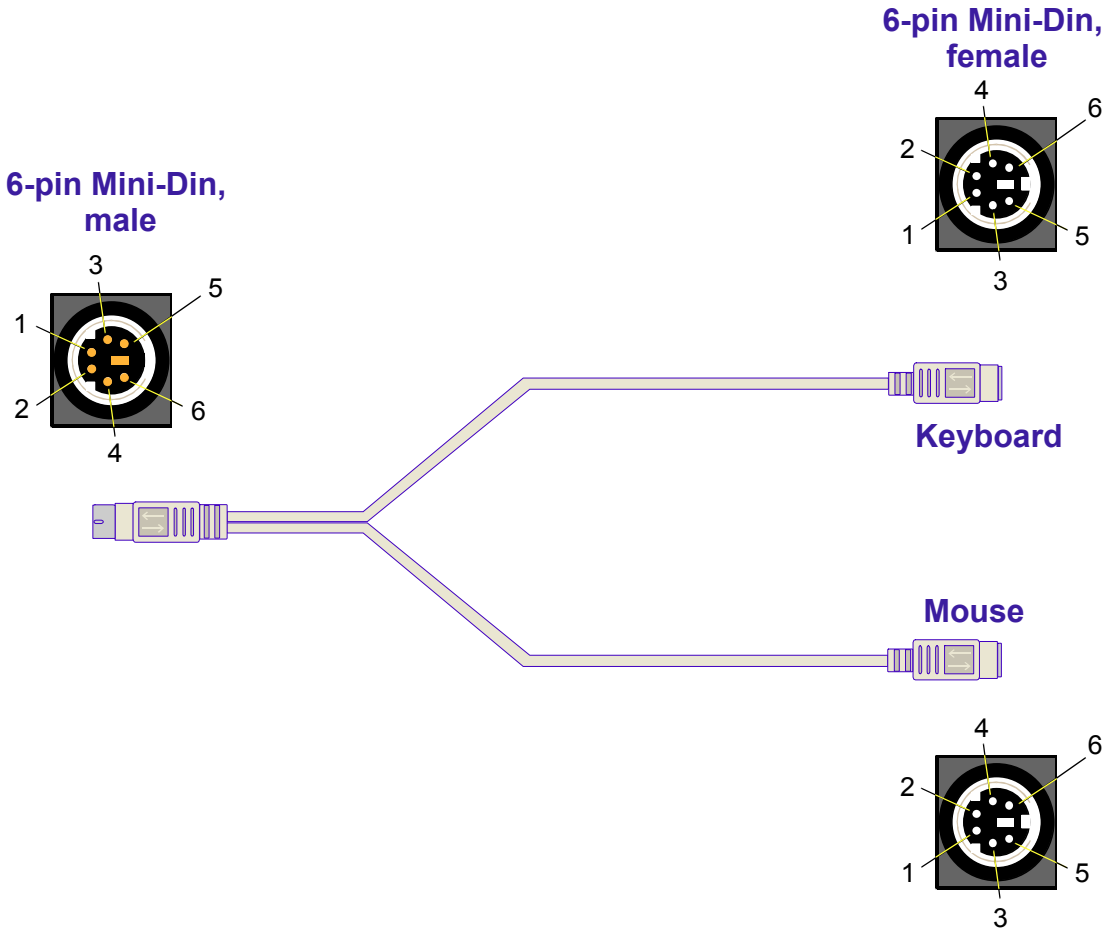
PIN	SIGNAL	DESCRIPTION	IN/OUT
1	KDATA	Keyboard data	I/O
2	MDATA	Mouse data	I/O
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	I/O
6	MCLK	Mouse clock	I/O

Note ...

The keyboard and mouse power supply (VCC) provides 500 mA contiunuous load current and a short-circuit protection (900 mA). All the signal lines are EMI filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector is available from *Kontron.*

Figure 2-3: Adapter for Connecting Mouse/Keyboard via PS/2



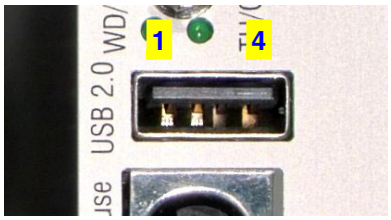
2.3.3 USB Interfaces

The CP306-V supports one USB 2.0 port on the front I/O and two USB 2.0 ports on the rear I/O interface. On the two rear I/O ports it is strongly recommended to use a cable below 3 metres in length for USB 2.0 devices. All ports are high speed, full speed, and low speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

One USB peripheral may be connected to the USB port. To connect more than one peripheral device to the USB port, an external hub is required.

The USB power supply provides 500 mA continuous load current a short-circuit protection (900 mA).

Figure 2-4: USB Connector J5



The following table indicates the pinout of the USB connector J5.

Table 2-10: USB Connector J5

PIN	SIGNAL	FUNCTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND signal	--

Note ...

The USB power supply to the USB connector provides 500 mA continuous load current a short-circuit protection (900 mA). All the signal lines are EMI filtered.

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2.3.4 Graphics Controller

The 855GME includes a highly integrated graphics accelerator delivering high performance 3D, 2D video capabilities. The internal graphics controller provides interfaces to a standard progressive scan monitor. These interfaces are only active when running in internal graphics mode. For the DVI interface a TMDS transmitter is used.

Integrated 2D/3D Graphics:

- 3D hyperpipelined architecture
- Full 2D hardware acceleration
- Intel 855GME D.V.M. Technology graphics core
- Integrated 350 MHz DAC
- Resolution up to 1600 x 1200 @ 100 Hz and 2048 x 1536 @ 75 Hz with 16-bit colors in analog mode (CRT)
- Integrated H/W Motion Compensation engines for software MPEG2 decode

2.3.4.1 Video Memory Usage

The 855GME chipset supports the new Dynamic Video Memory Technology (D.V.M.T.). This new technology ensures the most efficient use of all available memory for maximum 3D graphics performance. D.V.M.T. dynamically responds to application requirements allocating display and texturing memory resources as required.

The operating system requires a minimum of 1 MB and a maximum of 64 MB of system memory to support legacy VGA. System properties will display up to 64MB less than physical system memory available to the operating system.

The graphics driver for the Intel 855GME configuration will request up to 64 MB of memory from the OS. By reallocating memory to the system, memory is freed up for other applications when not needed by the graphics sub-system. Thus, efficient memory usage is ensured for optimal graphics and system memory performance.

2.3.4.2 Video Resolution

The 855GME has an integrated 350 MHz RAMDAC that can directly drive a progressive scan monitor up to a resolution of 1600x1200 @ 100 Hz and 2048 x 1536 @ 75 Hz.

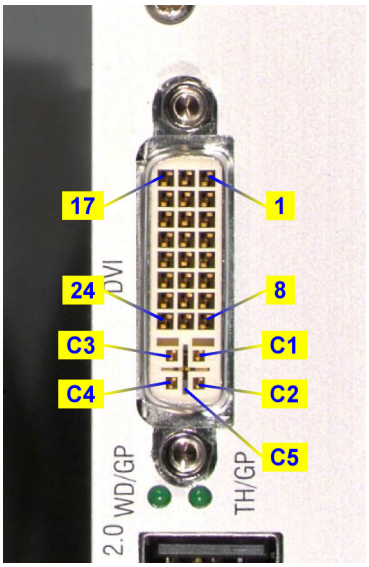
Table 2-11: Partial List of Display Modes Supported

DISPLAY MODE	COLOR RESOLUTION VERSUS HORIZONTAL FREQUENCY											
	8-BIT INDEXED				16-BIT				32-BIT			
	60	75	85	100	60	75	85	100	60	75	85	100
640 x 480	X	X	X	X	X	X	X	X	X	X	X	X
800 x 600	X	X	X	X	X	X	X	X	X	X	X	X
1024 x 768	X	X	X	X	X	X	X	X	X	X	X	X
1280 x 1024	X	X	X	X	X	X	X	X	X	X	X	X
1600 x 1200	X	X	X	X	X	X	X	X	X	X	X	X
1920 x 1440	X	X	X		X	X	X		X	X	X	
2048 x 1536	X	X			X	X						

2.3.4.3 DVI-I Connector J4

The DVI-I female connector J4 is used to connect an analog or digital monitor to the CP306-V board.

Figure 2-5: DVI-I Connector J4



The following table indicates the pinout of the DVI-I Connector J4.

Table 2-12: DVI-I Connector J4 Pinout

PIN	SIGNAL	DESCRIPTION	I/O	PIN	SIGNAL	DESCRIPTION	I/O
1	TMDS Data 2-	TMDS* Link -	O	2	TMDS Data 2+	TMDS* Link +	O
3	GND	Ground	--	4	Free	--	--
5	Free	--	--	6	DDC Clock	I^2C™ Clock	O
7	DDC Data	I^2C™ Data	I/O	8	Vsync	Vertical sync. TTL out	O
9	TMDS Data 1-	TMDS Link -	O	10	TMDS Data 1+	TMDS Link +	O
11	GND	Ground	--	12	Free	--	--
13	Free	--	--	14	VCC	Power +5 V max. 1.5A	--
15	GND	Ground	--	16	HPDETECT	Hot Plug Detect	I
17	TMDS Data 0-	TMDS Link -	O	18	TMDS Data 0+	TMDS Link +	O
19	GND	Ground	--	20	Free	--	--
21	Free	--	--	22	GND	Ground	--
23	TMDS Clock +	TMDS Link +	O	24	TMDS Clock -	TMDS Link -	O
C1	RED	Red video signal output	O	C2	GREEN	Green video signal output	O
C3	BLUE	Blue video signal output	O	C4	Hsync	Horizontal sync. TTL out	O
C5	GND	Ground	O				

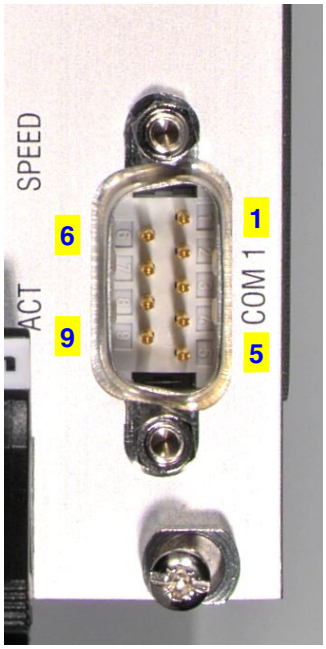
* TMDS = Transition Minimized Differential Signaling

2.3.5 Universal Serial Ports (UART)

2.3.5.1 Serial Port Interface COM1 and COM2

Two PC-compatible serial ports with TTL signal level are available on the CompactPCI rear I/O. These two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s. The COM2 port is only available on the CompactPCI rear I/O interface, the COM1 port can be switched in BIOS between the front panel and the rear I/O.

Figure 2-6: COM1 D-SUB Connector J15A



The following table indicates the pinout of theD-SUB Connector J15A.

Table 2-13: D-SUB Connector J15A Pinout

D-SUB 9	SIGNAL	DESCRIPTION	IN/OUT
1	DCD	Data carrier detect	I
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	GND	Signal ground	--
6	DSR	Data set ready	I
7	RTS	Request to send	O
8	CTS	Clear to send	I
9	RI	Ring indicator	I

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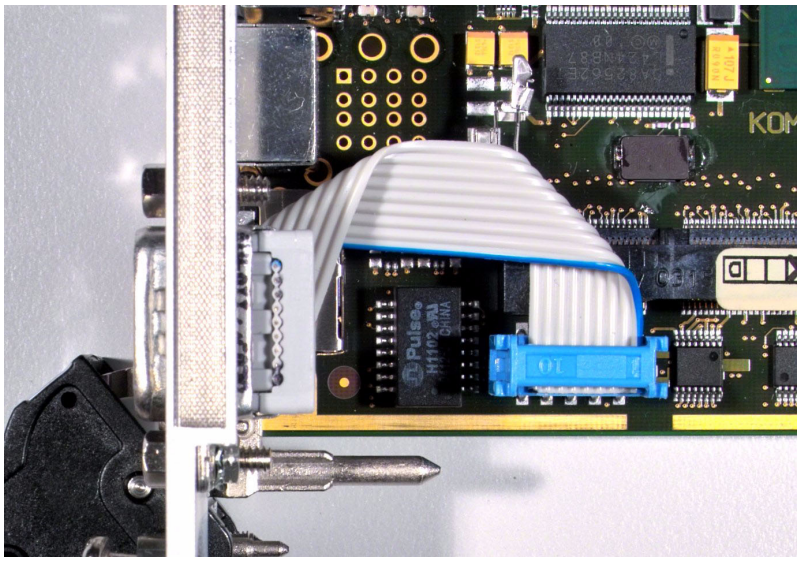
Figure 2-7: COM1 D-SUB Connector J15A Connected to Onboard Connector J15



2.3.5.2 Serial Port Configuration

Table 2-14: COM Port Configuration Matrix

BOARD	REAR I/O VARIANT	UART1	UART2
4HP board	No	--	--
4HP board	Yes	Rear I/O COM1	Rear I/O COM2
8HP board	No	Front panel COM1	--
8HP board	Yes	Rear I/O or front panel COM1	Rear I/O COM2

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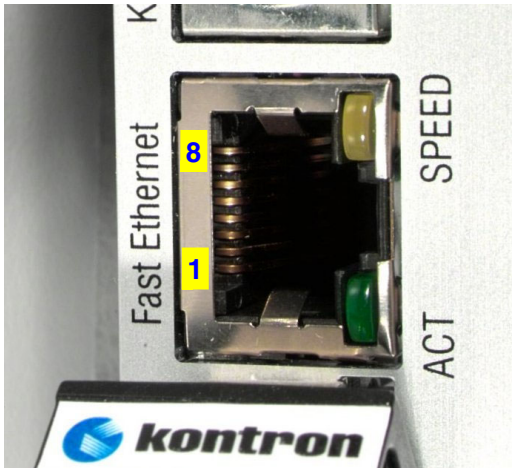
2.3.6 Fast Ethernet

The CP306-V board includes one 10Base-T/100Base-TX Ethernet port integrated within the ICH4 chipset (82559 style).

The Boot from LAN feature is supported; for details please refer to section 5.5, BIOS Features Setup, in chapter 5, CMOS Setup.

Figure 2-8: Fast Ethernet Controller J8



The Ethernet connector is realized as an RJ45 connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission. The Ethernet channel may be configured via the BIOS setting or the rear I/O Configuration Register for front I/O or rear I/O. The standard software configuration is front I/O.

Note ...

The maximum length of cabling over which the Ethernet transmission can operate effectively depends upon the transceiver in use.

RJ45 Connector J8 Pinout

The J8 connector supplies the 10Base-T/100Base-TX interfaces to the Ethernet controller.

Table 2-15: RJ45 Connector J8 Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
1	TX+	Transmit +	O
2	TX-	Transmit -	O
3	RX+	Receive +	I
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	I
7	NC	--	--
8	NC	--	--

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Ethernet LED Status

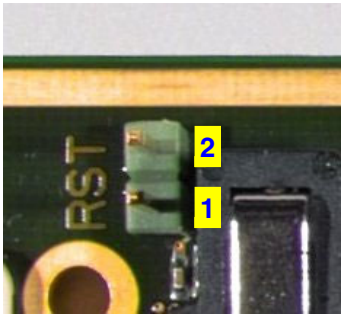
Green: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit, it means that either the computer is not sending or receiving network data, or the cable connection is faulty.

Orange: SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit, the connection is operating at 10Base-T.

2.3.7 Reset Connector J9

The CP306-V includes a reset connector J9 which is used to reset the system. If the CP306-V-IOIDE module is used with the CP306-V, this connector is routed to the reset button on the respective front panel.

Figure 2-9: Reset Connector J9



The following table indicates the pinout of the reset connector J9.

Table 2-16: Reset Connector J9 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	RST	Reset	I
2	GND	Ground	--

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2.3.8 EIDE Interface

The EIDE interface supports the following modes:

- Programmed I/O (PIO): CPU controls data transfer.
- 8237-style DMA: DMA offloads the CPU, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH4 ATA-100 logic can achieve read transfer rates of up to 100 MB/sec and write transfer rates up to 88 MB/sec.

There are two independent EIDE ports available. The primary port is connected to the 44-pin, 2-row male connector AT standard interface for 2.5” hard disks. The secondary EIDE port is a 40-pin, 2-row male connector AT standard interface for an EIDE hard disk.

Both EIDE ports provide support for two devices (one master and one slave). All hard disks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA) mode.

Note ...

Both EIDE ports support a maximum of two devices connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the hard disk manufacturer’s documentation.

Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must connect to the motherboard, the gray connector to the UltraDMA / 100 slave device and the black connector to the UltraDMA / 100 master device.

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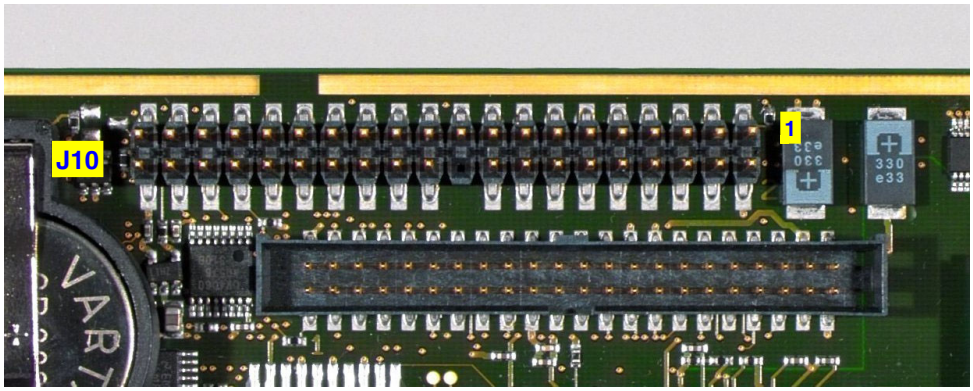
Figure 2-10: 40-Pin EIDE Connector J10



The following table sets out the pinout of the secondary EIDE connector J10, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm.

Table 2-17: 40-Pin EIDE Connector J10 Pinout

I/O	DESCRIPTION	SIGNAL	PIN	PIN	SIGNAL	DESCRIPTION	I/O
Out	Reset HD	IDERESET	1	2	GND	HD data 7	--
In/Out	HD data 7	HD7	3	4	HD8	HD data 8	I/O
In/Out	HD data 6	HD6	5	6	HD9	HD data 9	I/O
In/Out	HD data 5	HD5	7	8	HD10	HD data 10	I/O
In/Out	HD data 4	HD4	9	10	HD11	HD data 11	I/O
In/Out	HD data 3	HD3	11	12	HD12	HD data 12	I/O
In/Out	HD data 2	HD2	13	14	HD13	HD data 13	I/O
In/Out	HD data 1	HD1	15	16	HD14	HD data 14	I/O
In/Out	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	--	--	--
In	DMA request	IDEDRQ	21	22	GND	Ground signal	--
Out	I/O write	IOW	23	24	GND	Ground signal	--
Out	I/O read	IOR	25	26	GND	Ground signal	--
In	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
Out	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
In	Interrupt request	IDEIRQ	31	32	NC	--	--
Out	Address 1	A1	33	34	ATA100	Detect ATA100	I
Out	Address 0	A0	35	36	A2	Address 2	O
Out	HD select 0	HCS0	37	38	HCS1	HD select 1	O
In	LED driving	LED	39	40	GND	Ground signal	--

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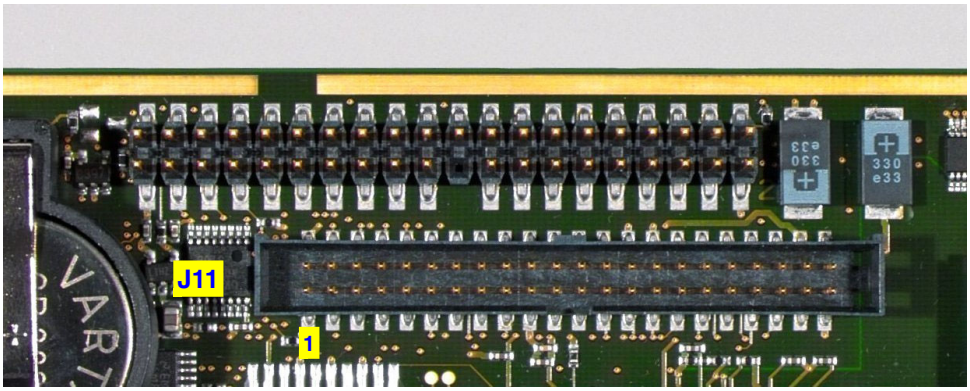
Figure 2-11: 44-Pin EIDE Connector J11



A 2.5” hard disk or Flash disk may be mounted directly onto the CP306-V board using the optional 44-pin connector J11. The maximum length of the cable that may be used is 35 cm.

Table 2-18: 44-Pin EIDE Connector J11 Pinout

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	N/C	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	N/C	--	--
O	Address 1	A1	33	34	ATA66	Detect ATA66	I
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	LED driving	LED	39	40	GND	Ground signal	--
--	5V power	VCC	41	42	VCC	5V power	--
--	Ground signal	GND	43	44	N/C	--	--

2.3.9 CompactPCI Bus Interface

The complete CompactPCI connector configuration comprises two connectors named J1 and J2.

Their function is as follows:

- J1: 32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2: has optional rear I/O interface functionality or 64-bit termination

The board is capable of driving up to seven CompactPCI slots, with individual arbitration and clock signals. In addition to standard CompactPCI system functionality, the CP306-V also supports hot swap capability which means that hot swappable boards can be removed from or installed in the system whilst it is running.

The CP306-V is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.3.9.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3 V and 5 V operation.

Color coded keys prevent inadvertent installation of a 5 V peripheral board into a 3.3 V slot. The CP306-V board may be ordered as either a 3.3 V or a 5 V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-19: Coding Key Colors

SIGNALING VOLTAGE	KEY COLOR
3.3 V	Cadmium Yellow
5 V	Brilliant Blue
Universal board (5V and 3.3V)	None

2.3.9.2 CompactPCI Connectors J1 and J2

The CP306-V is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Figure 2-12: CompactPCI Connectors J1 and J2

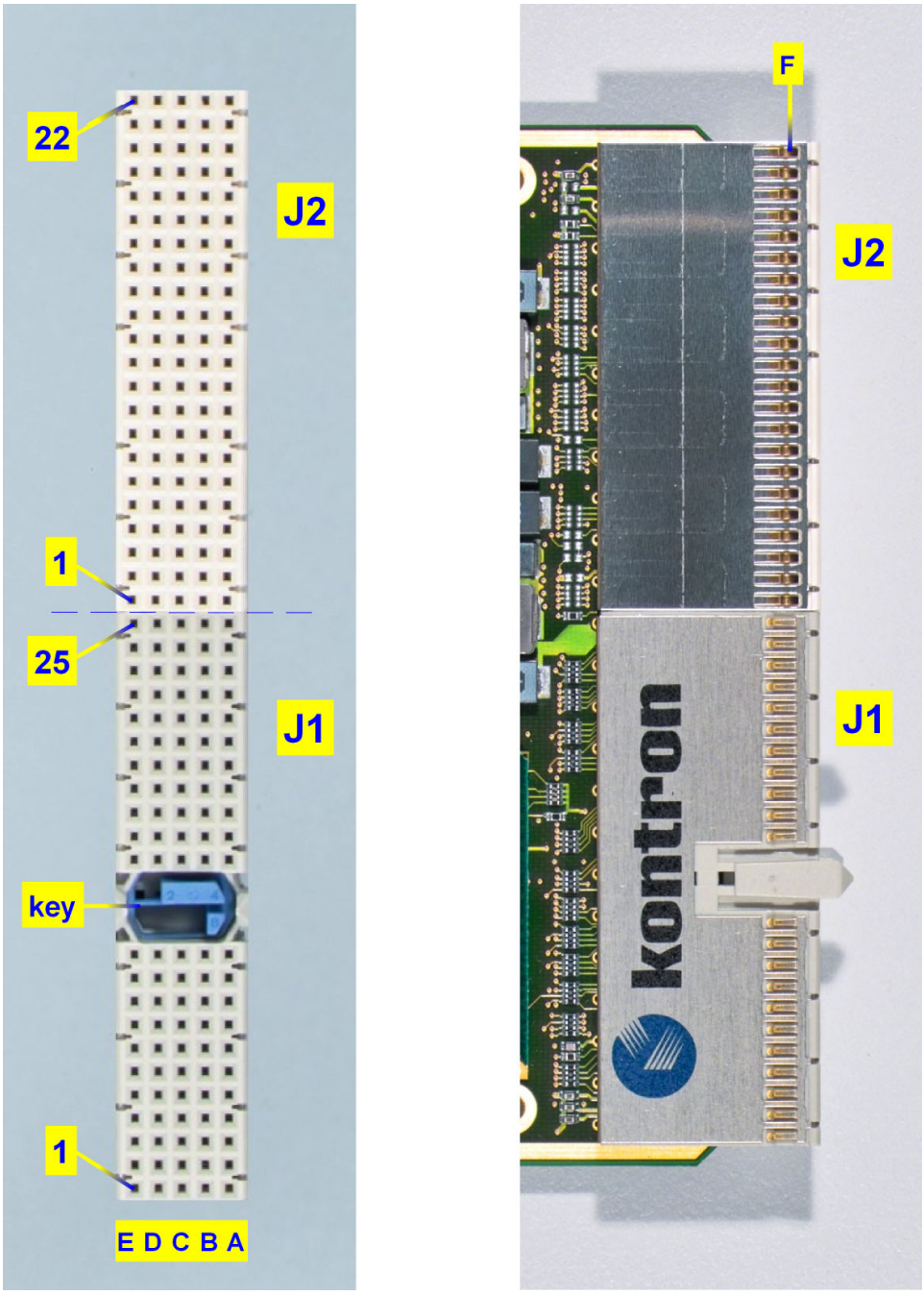


Table 2-20: CompactPCI Bus Connector J1 Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN#	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	DEVSEL	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL (OPEN)	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ0#	GND	3.3V	CLK0	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0	GND
4	IPMB PWR	GND	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND

Table 2-21: 64-bit CompactPCI Bus Connector J2 Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	TDN1	RDN1	RDP1	GND
20	CLK5	GND	TDP1	GND	RSV	GND
19	GND	GND	RSV	RSV	RSV	GND
18	RSV	RSV	RSV	GND	RSV	GND
17	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	RSV	RSV	DEG#	GND	RSV	GND
15	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND
4	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note ...

The 64-bit CompactPCI signals are not used on the board, but all 64 control signals are terminated to V(I/O).

The TDN1, RDN1, RDP1 and TDP1 signals are only available if the Fast Ethernet port is configured for rear I/O. For detailed information on the configuration of the Fast Ethernet port refer to chapter 5.6.4 Front RearI/O in the Phoenix BIOS Chapter.

Warning!

The pins C20, C21, D21, E21 must not be used for other purposes. Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2.3.10 Optional Rear I/O Interface on CompactPCI Connector J2

The CP306-V board provides optional rear I/O connectivity for special compact systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP306-V with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support on the system slot.

The CP306-V rear I/O provides the following interfaces (all signals are available on J2 only if the board is ordered with rear I/O functionality):

The CP306-V comes with the following features:

- 32-bit/33 MHz CompactPCI and rear I/O
- Two USB 2.0 ports
- One Fast Ethernet port without LED
- Primary EIDE Port with ATA100 (only ATA33 with CompactFlash)
- Two COM ports (TTL level)
- CRT VGA port
- Two fan control input
- One general purpose output
- Input for external backup battery
- PS/2 mouse and keyboard

Note ...

The pinout for the Ethernet, USB, COM, EIDE and VGA ports is identical to the CP302, CP303, CP303-V, CP304, and CP306 pinouts.

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2.3.10.1 Optional Rear I/O Interface on CompactPCI Connector J2

The CP306-V conducts a wide range of I/O signals through the rear I/O connector J2.

Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board.

Table 2-22: Rear I/O CompactPCI Bus Connector J2 Pinout

PIN	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	FANSENSE2	RES	+3.3V	GND
18	GND	KDAT	UV2-	UV4+	RTC Bat	+3.3V	GND
17	GND	KCLK	ROUT (GND)	PRST#	REQ6#	GNT6#	GND
16	GND	PMDAT	UV2+	DEG#	GND	UV4-	GND
15	GND	PMCLK	GOUT (GND)	FAL#	REQ5#	GNT5#	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE1 (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	IDE_PD[9]	1DCD	1RIN	GND
10	GND	IDE_PD[8]	IDE_RST#	1TXD	IDE_PD[10]	1RXD	GND
9	GND	IDE_PD[6]	IDE_PD[7]	IDE_PD[4]	IDE_PD[5]	IDE_PD[11]	GND
8	GND	IDE_PD[3]	IDE_PD[12]	IDE_PD[2]	GND	IDE_PD[1]	GND
7	GND	IDE_PD[14]	IDE_PD[0]	IDE_PD[15]	IDE_PDRQ#	IDE_PIOW#	GND
6	GND	IDE_PIOR	IDE_PIORDY	IDE_PDACK#	IDE_PD [13]	IDE_PIRQ14	GND
5	GND	IDE_PA[1]	GND	IDE_PA[0]	IDE_PA[2]	TH_GP/ SLP_S3	GND
4	GND	VIO	VCC	IDE_PCS1#	GND	IDE_PCS3#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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Legend for table on preceding page

IDE Signals

IDE	Primary IDE signals

Ethernet1

TDP1/TDN1	Transmit Differential Pair.
RDP1/RDN1	Receive Differential Pair.

USB ports

UV2+/-	USB data differential data signals
UV4+/-	USB data differential data signals

Serial Ports 1 and 2

S1	COM1 Serial port signals; TTL level
S2	COM2 Serial port signals; TTL level

PS/2 Ports

KDAT/KCLK	PS/2 Keyboard signals
PMDAT/PMCLK	PS/2 Mouse signals

CONTROL Signals

FANSENSE1/2	Schmitt Trigger fan tachometer inputs; TTL level
TH_GP/SLEP_S3	General purpose output, TTL level This signal indicates the sleep state of S3.

VGA CRT signals

ROUT	Red signal
GOUT	Green signal
BOUT*	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.

* Note that this signal (BOUT) appears twice in the rear I/O CompactPCI bus connector J2 pinout in order to provide compatibility with the CP302. Pin number B11 refers to the CP306-V and C13 refers to the CP302. The default configuration is CP306-V (B11).

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Reserved Signals

RES	Reserved (leave open)

2.3.10.2 Rear I/O Configuration

Rear I/O interfaces are only available on rear I/O versions of the board.

In order to implement the system rear I/O feature, a system slot rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

Ethernet Interface

Fast Ethernet signals are available on the front RJ45 connector and on the rear I/O interface.

The combination of both front and rear I/O is not supported. Both Fast Ethernet channels are decoupled, but enabled separately. It is not possible to operate both the rear and front I/O at the same time. Switching over from front to rear I/O or vice versa is effected under BIOS control without the need to plug/unplug Ethernet cables.

VGA CRT Interface

The VGA CRT signals are available on J2 if the board is ordered for rear I/O configuration. In this configuration the rear and front I/O CRT interfaces are active, but must not be used simultaneously. The 75 ohm termination resistor for the red, green and blue video signals are equipped on the CP306-V.

It is possible to use the front DVI interface for a digital device and the rear I/O CRT interface for an analog device at the same time to show independent screens.

Note ...

Both VGA CRT ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time. Doing so will result in poor signal quality.

Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board.

Serial Interface COM1 and COM2

The COM1 port can be switched via BIOS to the front panel or the rear I/O. The COM2 port can be used only on the rear I/O interface.

USB Interface

The CP306-V supports one USB 2.0 port on the front I/O and two USB 2.0 ports on the rear I/O interface.

Note ...

All three USB ports may be used at the same time. It is strongly recommended to use cables less than 3 metres in length for the rear I/O interfaces.

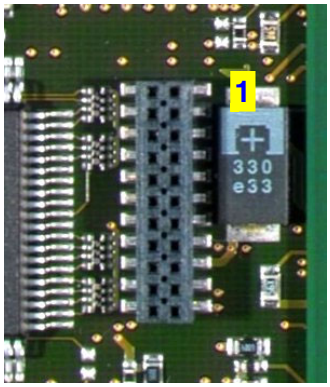
PS/2 Keyboard and Mouse

The keyboard and mouse ports can be used on the rear I/O interface or the front panel. It is not possible to connect two keyboards or two mouse devices at the same time on the front panel and the rear I/O.

2.3.11 I/O Extension Connector J13

On the Intel 855GME chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. To provide a flexible configuration of further low speed PC devices, e.g. Super I/O, IPMI or CAN controller, the LPC port is connected to the I/O extension connector. The I/O extension interface contains all the necessary signals to connect up to three LPC devices.

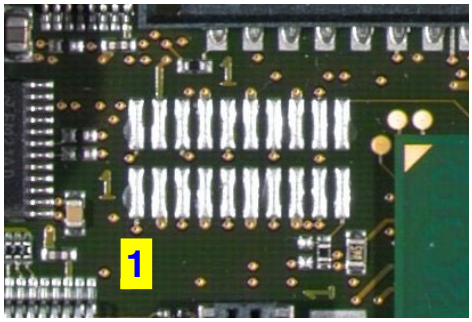
Figure 2-13: I/O Extension Connector J13



2.3.12 LVDS Connector J12 (Optional)

An LVDS display can be connected to the CP306-V via the optional LVDS connector J12. This interface contains all the necessary signals required to drive LVDS displays with a color depth of 6 bits.

Figure 2-14: LVDS Connector J12



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Chapter 3

Installation

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3. Installation

The CP306-V has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP306-V. *Kontron* assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note ...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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3.2 CP306-V Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP306-V in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP306-V in a system proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP306-V refer to Chapter 4. For the installation of CP306-V specific peripheral devices and rear I/O devices refer to the appropriate chapters in Chapter 3.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP306-V nor other system boards are physically damaged by the application of these procedures.

3. To install the CP306-V perform the following:
   1. Ensure that no power is applied to the system before proceeding.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   4. Fasten the front panel retaining screws (two on the 4HP version and four on the 8HP).
   5. Connect all external interfacing cables to the board as required.
   6. Ensure that the board and all required interfacing cables are properly secured.

1. The CP306-V is now ready for operation. For operation of the CP306-V, refer to appropriate CP306-V specific software, application, and system documentation.

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3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP306-V nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws (two on the 4HP version and four on the 8HP).
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

3.4 Hot Swap Procedures

The CP306-V supports hot swap operation on peripheral slots. The CP306-V itself is not hot swap capable. When installed in the system slot, it is capable of supporting peripheral board hot swapping. In any event, hot swap is also a function of the application running on the CP306-V.

3.5 Installation of CP306-V Peripheral Devices

The CP306-V is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

3.5.1 CompactFlash Installation

The CompactFlash socket supports all available CompactFlash ATA cards type I and type II.

Warning!

The CP306-V does not support removal and reinsertion of the CompactFlash storage card while the board is in a powered-up state. Connecting or disconnecting the CompactFlash cards while the power is on, which is known as "hot plugging", will result in irreparable damage to the system.

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3.5.2 USB Device Installation

The CP306-V supports all USB plug and play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.5.3 Rear I/O Device Installation

Rear I/O interfaces are only available on rear I/O versions of the board. In order to implement the system rear I/O feature, a system slot rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

3.5.4 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

3.5.5 Hard Disk Installation

The following information pertains to hard disks which may be connected to the CP306-V via normal cabling. To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware.

Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP306-V board.

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Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must connect to the motherboard, the gray connector to the UltraDMA/100 slave device, and the black connector to the UltraDMA/100 master device.

Some symptoms of incorrectly installed HDDs are:

- Hard disk drives are not auto-detected: may be a Master / Slave problem or a bad IDE cable. Contact your vendor.
- Hard Disk Drive Fail message at bootup: may be a bad cable or lack of power going to the drive.
- No video on bootup: usually means the cable is installed backwards.
- Hard drive lights are constantly on: usually means bad IDE cable or defective drives / motherboard. Try another HDD.
- Hard drives do not power up: check power cables and cabling. May also result from a bad power supply or IDE drive.

2. Initialize the software necessary to run the chosen operating system.

3.6 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® 95/98/ME, Windows® 2000, Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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4. Configuration

4.1 Jumper Description

4.1.1 Reset Jumper

Table 4-1: Reset Jumper

J9	DESCRIPTION
Open	***Reset is not active***
Closed	Reset is active

The default setting is indicated by using italic bold.

4.1.2 Clearing BIOS CMOS Setup

If the system does not boot (for example, due to wrong BIOS configuration, or wrong password setting) the CMOS setting may be cleared using Jumper JP1.

Procedure for clearing CMOS setting:

The system must be booted with the jumper in the closed position, then powered down again. The jumper is then reset back to the normal position, and the system is rebooted..

Table 4-2: Clearing BIOS CMOS Setup

JP1	DESCRIPTION
Open	***Normal boot using the CMOS settings***
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by using italic bold.

4.1.3 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated from the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table 4-3: Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C457, C89, C239	***Closed 470pF 2KV capacitors***	***Connectors are isolated to logic GND with three 470pF 2KV capacitors***
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by using italic bold.

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4.2 Interrupts

The CP306-V board uses the standard AT IRQ routing (8259 controller).

This interrupt routing of certain functions can be modified via the BIOS settings.

Table 4-4: Interrupt Setting

IRQ	PRIORITY	STANDARD FUNCTION
IRQ0	1	System Timer
IRQ1	2	Keyboard Controller
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	COM2
IRQ4	12	COM1
IRQ5	13	Watchdog
IRQ6	14	Floppy Disk Controller
IRQ7	15	Free reserved for COM3 or COM4
IRQ8	3	System Real Time Clock
IRQ9	4	PCI or ACPI
IRQ10	5	PCI
IRQ11	6	PCI
IRQ12	7	PCI or PS/2 mouse
IRQ13	8	Coprocessor error
IRQ14	9	Primary hard disk
IRQ15	10	Secondary hard disk
NMI		Watchdog

Note ...

Selecting legacy USB support in the BIOS will initiate an emulation of a PS/2 keyboard. This emulation uses a cyclic SMI interrupt whereby the latency of the interrupt handler may by up to 250 µsec. The BIOS and the CPU speed are the primary influences concerning the increased latency. The latency is not consistent with regards to occurrence or duration.

Since the SMI is the highest IRQ, other IRQ routines may experience erratic latency. Should this interfere with the application requirements, turn off this option in the BIOS or disable the SMIs in the start-up boot code.

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4.3 Onboard PCI Interrupt Routing

The ICH4 provides up to 8 PCI interrupt inputs. The table below describes the connection of these IRQ signals.

For more information please see the INTEL ICH4 datasheet.

Table 4-5: PCI Interrupt Routing

ICH4 IRQ INPUT	PCI DEVICE	FUNCTION INTERNAL ICH4
PIRQA	Free	USB A controller
PIRQB	CPCI IRQA	AC97 + MODEM + SMBUS
PIRQC	Free	USB C controller
PIRQD	Free	USB B controller
PIRQE	Free	ICH4 LAN controller
PIRQF	CPCI IRQB	Free
PIRQG	CPCI IRQC	Free
PIRQH	CPCI IRQD	USB 2.0 controller

4.4 Memory Map

The CP306-V board uses the standard AT ISA memory map.

4.4.1 Memory Map for the 1st Megabyte

The following table sets out the memory map for the first megabyte.

Table 4-6: Memory Map for the 1st Megabyte

MEMORY RANGE	SIZE	FUNCTION
0xE0000 – 0xFFFFF	128 k	BIOS implemented in FWH Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCD000 – 0xCFFFF	12 k	Free
0xC0000 – 0xCCFFF	52 k	BIOS of the VGA card.
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM as follows: CGA video: 0xB8000-0xBFFFF Monochrome video: 0xB0000-0xB7FFF EGA/VGA video: 0xA0000-0xAFFFF
0x000000 – 0x9FFFF	640 k	DOS reserved memory space

Note ...

The 1 MB FLASH extension is mapped in the extended memory area e.g. 0xFFF00000–0xFFFFFFFF. The Flash address range can be configured by the ICH4 chip.

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4.4.2 I/O Address Map

The following table sets out the memory map for the I/O memory. The shaded table cells indicate CP306-V specific registers.

Table 4-7: I/O Address Map

ADDRESS	DEVICE
000,00F	DMA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A1	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Hard disk secondary
1F0,1FF	Hard disk primary
278,27F	Parallel port LPT2
280	Watchdog trigger
282	Watchdog timer
284	Watchdog, CPCI IRQ routing
286	I/O status
287	I/O configuration
288	Board version
289	Hardware index
28B	Logic index
28D	LED control
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk + Super-I/O #1 Com.
3F8,3FF	Serial port COM1

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4.5 Special Registers Description

The following registers are special registers which the CP306-V uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.

Note ...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.5.1 Watchdog

The CP306-V has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the watchdog timer within a set time period results in a system reset, NMI or an interrupt. This can be configured via the register 0x284.

To enable the watchdog bit ”4” of the register 0x282 must be set. If the watchdog is enabled via bit ”4” this bit cannot later be cleared.

With a write access to the register 0x280 the watchdog is retriggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware.

The watchdog can be configured in several modes, one of which is the dual stage configuration. If the NMI and the reset configuration bit are set (0x284 = 0x84) the watchdog has two stages. The first stage timeout generates an NMI interrupt. If the NMI handler does not reconfigure the watchdog, the watchdog switches to the second stage and generates a master reset after the configured timeout elapses.

4.5.2 Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

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4.5.3 Watchdog Timer

Table 4-8: Watchdog Timer

REGISTER NAME		Watchdog Timer						ACCESS	
ADDRESS		0x282						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	WDEN	WDT3	WDT2	WDT1	WDT0
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0 1 2 3	WDT[3:0]		Timeout Period: Bits: 3 2 1 0 Setting: 0 0 0 0 = 0 = 000.125 sec 0 0 0 1 = 1 = 000.250 sec 0 0 1 0 = 2 = 000.500 sec 0 0 1 1 = 3 = 001 sec 0 1 0 0 = 4 = 002 sec 0 1 0 1 = 5 = 004 sec 0 1 1 0 = 6 = 008 sec 0 1 1 1 = 7 = 016 sec 1 0 0 0 = 8 = 032 sec 1 0 0 1 = 9 = 064 sec 1 0 1 0 = 10 = 128 sec 1 0 1 1 = 11 = 256 sec 1 1 0 0 = 12 = res. 1 1 0 1 = 13 = res. 1 1 1 0 = 14 = res. 1 1 1 1 = 15 = res.						
4	WDEN	0	Watchdog timer disabled						
		1	Watchdog timer enabled ***Note ...*** Once the watchdog timer is enabled it cannot be disabled except by resetting the system.						
5		0	Reserved						
6		0	Reserved						
7		0	Reserved						

4.5.4 Watchdog, CompactPCI Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal. If the watchdog timer fails, it can generate three independent hardware events: reset, NMI and IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Note ...

To enable the dual stage watchdog the NMI and the reset bit must be set. At the first stage the watchdog generates an NMI and at the second stage the system will be reset.

Table 4-9: Watchdog, CompactPCI Interrupt Configuration Register

REGISTER NAME		Interrupt Configuration Register						ACCESS	
ADDRESS		0x284						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WNMI	CFNMI	CFIRQ	CEIRQ	CDIRQ	WRST	WIRQ	Res.
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0		0	Reserved						
1	WIRQ	0	Disable Watchdog IRQ5 routing						
		1	Enable Watchdog IRQ5 routing						
2	WRST	0	Disable Watchdog hardware reset						
		1	Enable Watchdog hardware reset						
3	CDIRQ	0	Disable CPCI derate signal to IRQ5 routing						
		1	Enable CPCI derate signal to IRQ5 routing						
4	CEIRQ	0	Disable CPCI enum signal to IRQ5 routing						
		1	Enable CPCI enum signal to IRQ5 routing						
5	CFIRQ	0	Disable CPCI fail signal to IRQ5 routing						
		1	Enable CPCI fail signal to IRQ5 routing						
6	CFNMI	0	Disable CPCI fail signal to NMI routing						
		1	Enable CPCI fail signal to NMI routing						
7	WNMI	0	Disable Watchdog NMI routing						
		1	Enable Watchdog NMI routing						

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4.5.5 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not retriggered within the previously set time period, the bit is set to ”0” and the watchdog LED lights. The fail signal is an output of the power supply and indicates a power supply failure. For the description of the derate and enumeration signals please see the interrupt routing register.

Table 4-10: I/O Status Register

REGISTER NAME		I/O Status Register						ACCESS	
ADDRESS		0x286						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WST	Res.	Res.	Res.	CSLOT	CENUM	CFAIL	CDER
DEFAULT		1	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	CDER	0	Indicates power derating (CPCI DEG signal)						
		1	Power normal						
1	CFAIL	0	Indicates a power supply failure (CPCI FAIL signal)						
		1	Power normal						
2	CENUM	0	Indicates the insertion or removal of a hot swap system board (CPCI ENUM)						
		1	No hot swap event						
3	CSLOT	0	Indicates that the board is installed in a system slot						
		1	Indicates that the board is installed in a peripheral slot						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7	WST	0	Indicates that a Watchdog timeout has occurred						
		1	Indicates that no Watchdog timeout has occurred						

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4.5.6 I/O Configuration Register

The I/O configuration register holds a series of bits defining the onboard configuration for the general purpose LEDs.

Table 4-11: I/O Configuration Register

REGISTER NAME		I/O Configuration Register						ACCESS	
ADDRESS		0x287						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	DBIOS	ELED1	ELED0	Res.	Res.	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0	Res.	0	Reserved
		1	
1	Res.	0	Reserved
		1	
2	Res.	0	Reserved
		1	
3	Res.	0	Reserved
		1	
4	ELED0 (WD/GP)	0	Enable LED0 for watchdog
		1	Enable LED0 for GP
5	ELED1 (TH/GP)	0	Enable LED1 for over temperature
		1	Enable LED1 for GP
6	DBIOS	0	Default boot from onboard FWH
		1	Boot from IDE module FWH
7	Res.	0	Reserved
		1	

4.5.7 Board Version

This register describes the hardware and the board version. The content of this register is unique for each Kontron CompactPCI board.

Table 4-12: Board ID Register

REGISTER NAME	Board Version						ACCESS	
ADDRESS	0x288						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	0	1	0	0	0	0	0	0

4.5.8 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value 0 and will be incremented with each change in hardware as development continues.

Table 4-13: Hardware Index Register

REGISTER NAME	Hardware Index						ACCESS	
ADDRESS	0x289						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	HWI7	HWI6	HWI5	HWI4	HWI3	HWI2	HWI1	HWI0
DEFAULT	0	0	0	0	0	0	0	0

4.5.9 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

Table 4-14: Logic Version Register

REGISTER NAME	Logic Version						ACCESS	
ADDRESS	0x28B						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
DEFAULT	0	0	0	0	0	0	0	0

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4.5.10 LED Control

With the LED Control register the LED on the front panel can be switched on and off.

Table 4-15: LED Control Register

REGISTER NAME		LED Control Register						ACCESS	
ADDRESS		0x28D						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	Res.	Res.	LED1	LED0
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	LED0 (WD/GP)	0	LED off						
		1	LED on						
1	LED1 (TH/GP)	0	LED off						
		1	LED on						
2		0	Reserved						
3		0	Reserved						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7		0	Reserved						

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Chapter 5

Phoenix BIOS

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5. Phoenix BIOS

5.1 The Setup Guide

With the PhoenixBIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off.

Note ...

The menus shown here are from a typical system. The actual menus displayed on your screen may be quite different and depend on the hardware and features installed in your computer. For more accurate information about your BIOS Setup program, consult your system manual or contact the manufacturer.

5.1.1 Introduction to Setup

This manual describes the Phoenix BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off. A special feature of Kontron's CompactPCI boards is that all setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Phoenix BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intelx86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O sub-systems.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

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5.1.2 The Main Menu

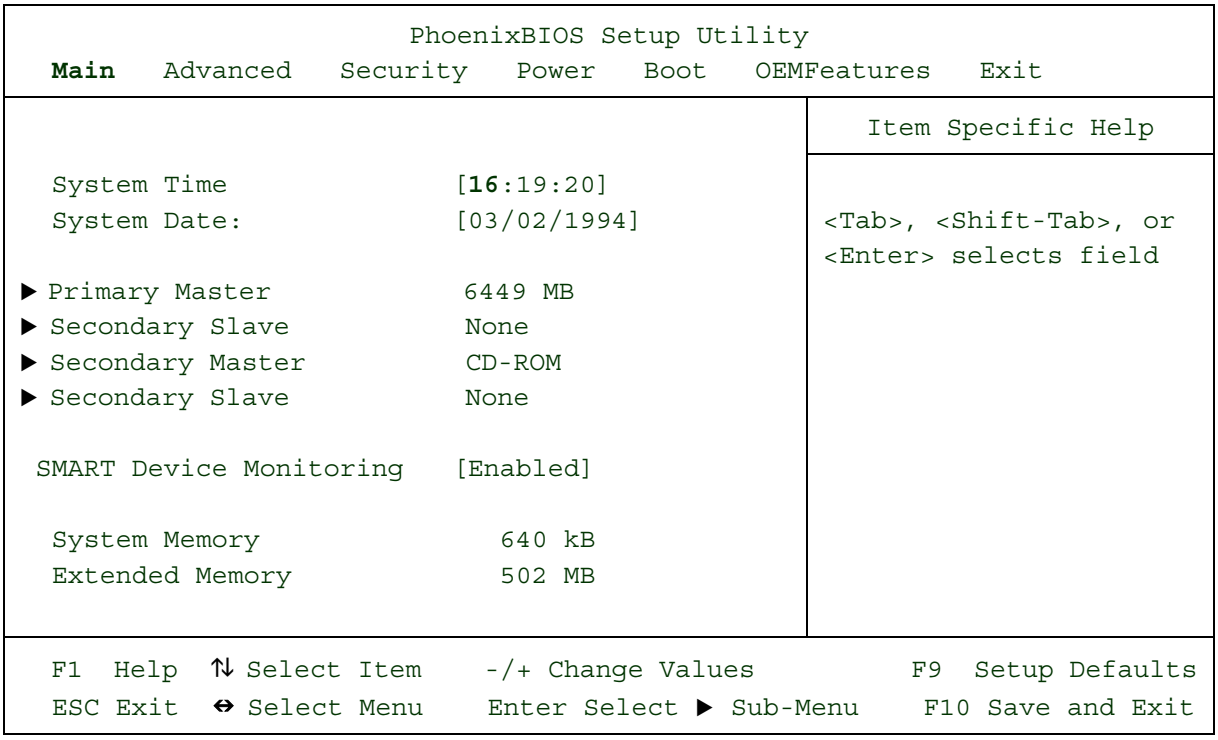
To start the ***Phoenix*BIOS** Setup utility:

Turn on or reboot your system. PhoenixBIOS displays this message:

Press <F2> to enter SETUP

Pressing <F2> displays the Main Menu, which looks like this:

Figure 5-1: Main Menu - Screen Display



5.1.3 The Menu Bar

The Menu Bar at the top of the window lists these selections:

Table 5-1: The Menu Bar

MENU	PURPOSE
Main	Basic system configuration
Advanced	Use to set the Advanced Features available on your system's chipset
Security	Use this menu to set the User and Supervisor Passwords and the Backup and Virus Check Reminders.
Power	Configuration of Power Management features
Boot	Boot sequence configuration
OEMFeatures	Configuration of special board features
Exit	Exits the current menu

Use the left and right (->, <-) arrow keys to make a selection.

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See the section below, "Exiting Setup" for a description on exiting the Main Menu.

5.1.4 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates

Table 5-2: The Legend Bar

KEY	FUNCTION
<F1> or <Alt-H>	General Help window (See below).
<Esc>	Exit this menu.
⇔ arrow keys	Select a different menu.
⇅ arrow keys	Move cursor up and down.
<Tab> or <Shift-Tab>	Cycle cursor in the Time and Date field.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F5> or <->	Select the Next Lower Value for the field.
<F9>	Load the Default Configuration values for the complete BIOS.
<F10>	Save and exit.
<Enter>	Execute Command or Select *P* sub-menu.
<Alt-R>	Refresh screen.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub-menu you want. Then press **<Enter>**.
A pointer ► marks all sub-menus.

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5.1.5 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

5.1.6 The General Help Window

Pressing **<F1>** or **<Alt-H>** on any menu brings up the General Help window that describes the legend keys and their alternates:

```
                        General Help

Setup changes system behavior by modifying the BIOS
Configuration parameters. Selecting incorrect values
may cause system boot failure; load Setup Default values
to recover.

<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>, or <Space> selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with a ▶,
<Enter> also displays an option list on some fields.

<F9> loads factory-installed Setup Default values.
<F10> saves and exits.

<ESC> or <Alt-X> exits Setup: in sub-menus, pressing these
keys returns to the previous menu.

<F1> or <Alt-H> displays General Help (this screen).

                          [Continue]
```

The scroll bar on the right of any window indicates that there is more than one page of information in the window. Use **<PgUp>** and **<PgDn>** to display all the pages. Pressing **<Home>** and **<End>** displays the first and last page. Pressing **<Enter>** displays each page and then exits the window.

Press **<Esc>** to exit the current window.

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5.1.7 Main Menu Selections

You can make the following selections on the Main Menu itself. Use the sub-menus for other selections.

Table 5-3: Main Menu Selections

FEATURE	OPTIONS	DESCRIPTION
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
SMART Device Monitoring	Disabled Enabled	Turns on Self-Monitoring Analysis Reporting Technology, which monitors the condition of the hard drive and reports when a catastrophic IDE failure is about to happen.

5.1.8 Master and Slave Sub-Menus

The **Master** and **Slave** sub-menus accessed from the Main Menu control these types of devices:

- Hard-disk drives
- Removable-disk drives such as Zip drives
- CD-ROM drives

*Phoenix*BIOS 4.0 supports up to two **IDE disk adapters**, called **primary** and **secondary** adapters. Each adapter supports one **master drive** and one optional **slave drive** in these possible combinations:

- 1 Master
- 1 Master, 1 Slave
- 2 Masters
- 2 Masters, 1 Slave
- 2 Masters, 2 Slaves

There is one IDE connector for each adapter on your machine, usually labeled "Primary IDE" and "Secondary IDE." There are usually two connectors on each ribbon cable attached to each IDE connector. In a two drive configuration, the order of placement of Device 0 and Device 1 on the ATA interface cable is not significant to the operation of the interface. If only a single device is attached via the ATA interface to a host, it is recommended that the host and the device be placed at the two ends of the cable.

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If you need to change your drive settings, selecting one of the Master or Slave drives on the Main Menu displays a sub-menu, as follows:-

Figure 5-2: Master/Slave Sub-Menu - Screen Display

```
                    PhoenixBIOS Setup Utility
        Main
```

Primary Master		Item Specific Help
Type:	[**User**]	User = you enter parameters of hard-disk installed at this connection Auto = auto types hard-disk drive installed here 1-39 = you select predetermined type of hard-disk drive installed here CD-ROM = a CD-ROM drive is installed here ATAPI Removable = removable disk drive is installed here.
CHS Format		
Cylinders:	[13328]	
Heads:	[15]	
Sectors	[63]	
Maximum Capacity:	6449 MB	
LBA Format		
Total Sectors	40031712	
Maximum Capacity	20496MB	
Multi Sector Transfer;	[16 Sectors]	
LBA Mode Control:	[Enabled]	
32-bit I/O:	[Enabled]	
Transfer Mode:	[Fast PIO 4]	
Ultra DMA Mode	[Enabled]	

```
F1  Help    ⇅ Select Item    -/+ Change Values        F9  Setup Defaults
ESC Exit    ⇔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu. Use the following chart to configure the hard disk.

Table 5-4: Master/Slave Sub-Menu Options

FEATURE	OPTIONS	DESCRIPTION
Type	None User Auto IDE Removable CD-ROM ATAPI Removable other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = You supply the hard-disk drive information in the following fields. Auto = Autotyping, the drive itself supplies the correct drive information. IDE Removable = Removable read-and-write media (e.g., IDE Zip drive). CD-ROM = Readable CD-ROM drive. ATAPI Removable = Read-and-write media (e.g., LS120)
Cylinders	0 to 65,535	Number of cylinders
Heads	1 to 16	Number of read/write heads
Sectors	0 to 63	Number of sectors per track
Multi-Sector Transfers	Disabled 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block.
LBA Mode Control	Enabled Disabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors.
32-Bit I/O	Enabled Disabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO3/DMA1 FPIO4/DMA2	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Ultra DMA Mode	Disabled Mode 0 up to Mode 5	Selects the Ultra DMA mode used for moving data to/from the drive.

When you enter Setup, the Main Menu usually displays the results of **Autotyping** information each drive provides about its own parameters (e.g., cylinders, heads, and sectors)–and how the drives are arranged as Masters or Slaves on your machine.

Some older drives, however, do not use Autotyping and require selecting type User and entering a pre-defined fixed-disk type value (e.g., 1 to 39) or specifying the drive parameters separately with the User type selected. You can find the correct parameters for hard-disk drives in the drive manual or written on the casing of the drive itself.

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Note ...

- Exiting this menu keeps your selections but loses internal autotyping information, which may not be selected. If you exit this menu and re-enter it, press <Enter> on Autotype again to restore the Autotype information.
- Do not attempt to change these settings unless you have an older drive that does not support autotyping.
- Before changing the contents of this menu, **write them down**. Once you have established correct parameters for your drive, **write them down and store them in a safe place** (e.g., tape them to the disk drive) for use in case these values are lost in CMOS or if autotyping fails. If these hard-disk parameters are not correctly entered in CMOS, you cannot access the data on your drive.

Warning!

Incorrect settings can cause your system to malfunction. To correct mistakes, return to Setup and restore the Setup Defaults with <F9> and re-enter the correct drive parameters.

5.2 The Advanced Menu

Selecting "Advanced" from the menu bar on the Main Menu displays a menu like this:

Figure 5-3: Advanced Menu - Screen Display

```
                    PhoenixBIOS Setup Utility
 Main    Advanced    Security    Power    Boot    OEM Features    Exit

                                                  Item Specific Help

                  Setup Warning
Setting items on this menu to incorrect values
may cause your system to malfunction.

▶ Advanced Chipset Control
▶ PCI/PNP Configuration
▶ Memory Cache
▶ I/O Device Configuration
▶ Keyboard Features
▶ Miscellaneous

 F1  Help   ⇅ Select Item   -/+ Change Values      F9  Setup Defaults
 ESC Exit   ⇔ Select Menu   Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use the legend keys to make your selections and exit to the Main Menu.

Warning ...

Incorrect settings can cause your system to malfunction. To correct mistakes, return to Setup and restore the Setup Defaults with <F9>.

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5.2.1 Advanced Chipset Control

Figure 5-4: Advanced Chipset Control - Screen Display

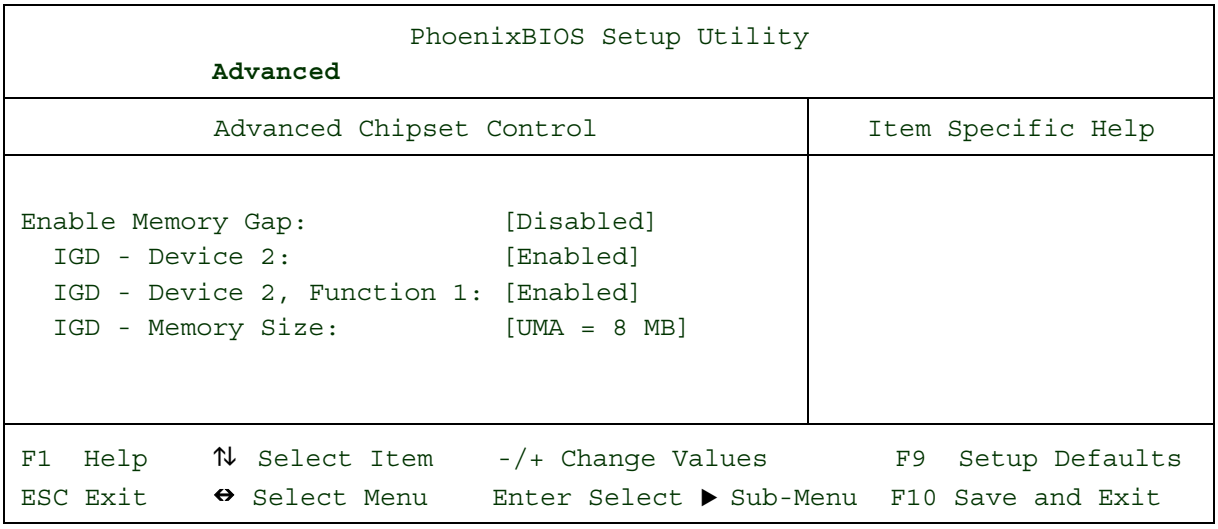

Table 5-5: Advanced Chipset Control Options

FEATURE	OPTIONS	DESCRIPTION
Enable Memory Gap	Disabled Extended (Enabled)	Allows enabling a 1 MB memory gap for add-on cards at 15 MB.
IGD - Device 2	Disabled Enabled	Enable/Disable the Internal Graphics Device.
IGD - Device 2, Function 1	Disabled Enabled	Enable/Disable Function 1 of the Internal Graphics Device by setting item to the desired value.
IGD - Memory Size	UMA = 1 MB UMA = 8 MB UMA = 16 MB UMA = 32 MB	Select the amount of legacy video memory that the Internal Graphics Device will use.

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5.2.2 PCI/PNP Configuration

Figure 5-5: PCI/PNP Configuration - Screen Display

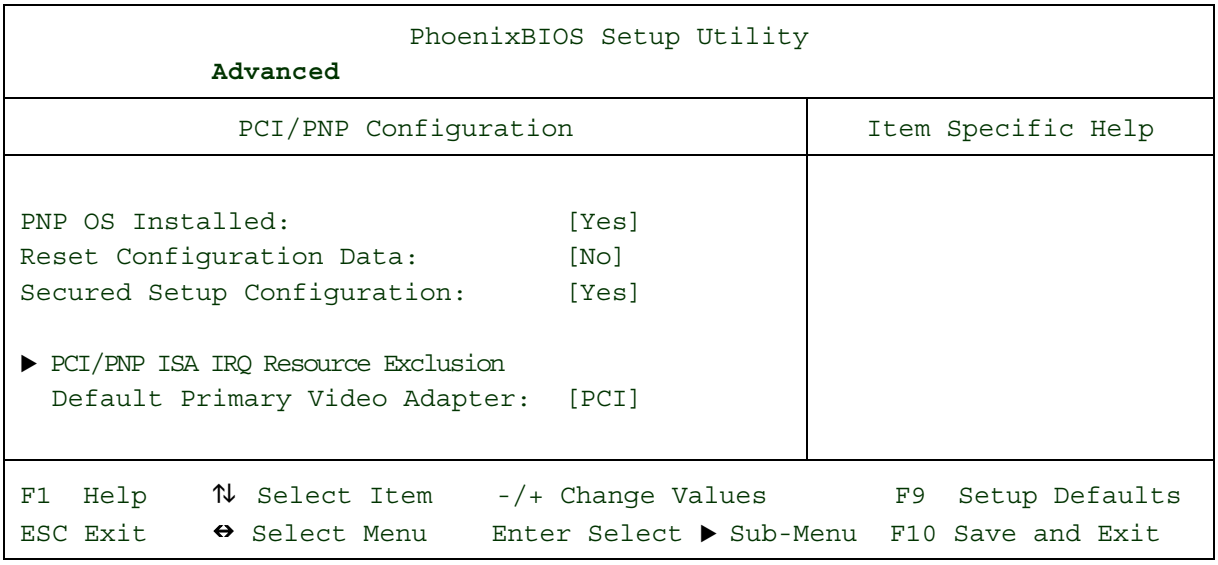

Table 5-6: PCI/PNP Configuration Options

FEATURE	OPTIONS	DESCRIPTION
PNP OS Installed	No Yes	Select the operating system installed on your system which you will use most commonly. Note: An incorrect setting can cause some operating systems to display unexpected behavior.
Reset Configuration Data	No Yes	Select Yes if you want to clear the Extended System Configuration Data (ESCD) area.
Secured Setup Configuration	No Yes	Yes prevents a Plug and Play OS from changing system settings.
Default Primary Video Adapter	PCI AGP	Select PCI to have a PCI video card, if installed, used for the boot display device. Select AGP to have an AGP video card, if installed, used for the boot display device. If no AGP card is present, the Integrated Graphics Device (IGD) will become to boot display device.

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5.2.2.1 PCI/PNP ISA IRQ Resource Exclusion

Figure 5-6: PCI/PNP ISA IRQ Resource Exclusion - Screen Display

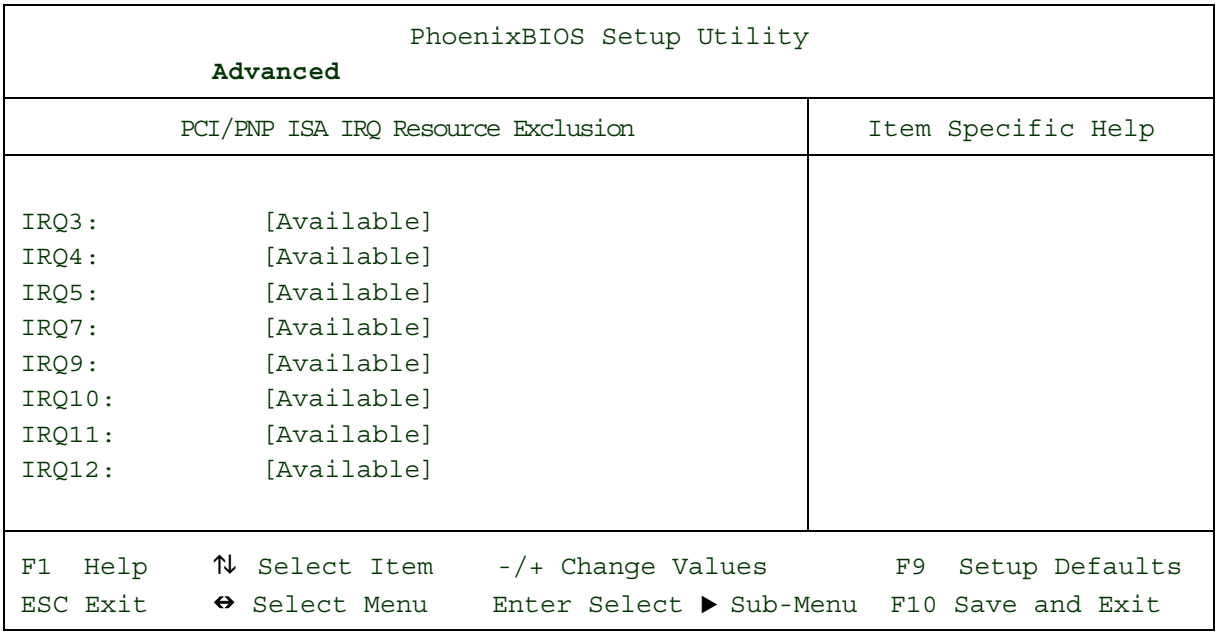

Table 5-7: PCI/PNP ISA IRQ Resource Exclusion Options

FEATURE	OPTIONS	DESCRIPTION
IRQ3-IRQ12	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.

Note ...

IRQ9 is used for SCI in ACPI mode. Do not use IRQ9 for legacy ISA devices.

5.2.3 Memory Cache

Enabling **cache** saves time for the CPU by holding data most recently accessed in regular memory (dynamic RAM or DRAM) in a special storage area of static RAM (SRAM), which is faster. Before accessing regular memory, the CPU first accesses the cache. If it does not find the data it is looking for there, it accesses regular memory. Selecting "Memory Cache" from the Main menu displays a menu like the one shown here. The actual features displayed depend on your system's hardware.

Figure 5-7: Memory Cache - Screen Display

```
                    PhoenixBIOS Setup Utility
          Advanced
+-------------------------------+-------------------------------+
|        Memory Cache           |      Item Specific Help       |
|                               |                               |
| Memory Cache                  | Sets the state of the         |
| Cache System BIOS Area:       | memory cache.                 |
| Cache Video BIOS Area:        |                               |
| Cache Base 0-512k:            |                               |
| Cache Base 512k-640k:         |                               |
| Cache Extended Memory Area:   |                               |
| Cache D000 - D3FF:            |                               |
| Cache D400 - D7FF:            |                               |
| Cache D800 - DBFF:            |                               |
| Cache DC00 - DFFF:            |                               |
|                               |                               |
+-------------------------------+-------------------------------+
 F1  Help   ↑↓ Select Item   -/+ Change Values     F9  Setup Defaults
 ESC Exit   ↔ Select Menu    Enter Select ▶ Sub-Menu   F10 Save and Exit
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu. Use this chart to configure the memory cache.

Table 5-8: Memory Cache Configuration Options

FEATURE	OPTIONS	DESCRIPTION
Memory Cache	Disabled Enabled	Sets the state of the memory cache.
Cache System BIOS area	Write Protect Uncached	Controls caching of system BIOS area.
Cache Video BIOS area	Write protect Uncached	Controls caching of video BIOS area.
Cache Base 0- 512k	Uncached Write Through Write Protect Write Back	Controls caching of 512k memory.
Cache Base 512k-640k	Uncached Write Through Write Protect Write Back	Controls caching of 512k- 640k base memory.
Cache Extended Memory Area	Uncached Write Through Write Protect Write Back	Controls caching of system memory above one megabyte.
Cache segments D000-DFFF	Disabled Write Through Write Protect Write Back	Controls caching of individual segments of memory usually reserved for shadowing system or option ROMs. Disabled: This block is not cached Write Through: Writes are cached and sent to main memory at once. Write Protect: Writes are ignored Write Back: Writes are cached, but not sent to main memory until necessary

Warning!

Incorrect settings can cause your system to malfunction. To correct mistakes, return to Setup and restore the Setup Defaults with <F9>.

5.2.4 I/O Device Configuration Menu

The CPU communicates with external devices such as printers through devices called **Input/Output (I/O) ports** such as serial and parallel ports. These I/O devices require the use of system resources such as I/O addresses and interrupt lines. If these devices are Plug and Play, either the BIOS can allocate the devices during POST, or the operating system can do it. If the I/O devices are not Plug and Play, they may require manually setting them in Setup.

On some systems, the **chipset** manages the communication devices. Other systems have, instead, a separate **I/O chip** on the motherboard for configuring and managing these devices.

Many systems allow you to control the configuration settings for the I/O ports. Select "I/O Device Configuration" on the Advanced Menu to display this menu and specify how you want to configure these I/O Devices:

Figure 5-8: I/O Device Configuration Menu - Screen Display

```
                    PhoenixBIOS Setup Utility
            Advanced
```

I/O Device Configuration		Item Specific Help
Local Bus IDE Adapter:	[Both]	
USB Controller 3:	[Enabled]	
USB Controller 2 and 3:	[Enabled]	
USB Controller 1, 2 and 3:	[Enabled]	
USB EHCI Host Controller:	[Enabled]	
Legacy USB Support:	[Enabled]	
Onboard LAN Controller:	[Enabled]	
COM Port 1:	[Enabled]	
	[3F8]	
Interrupt:	[IRQ4]	
COM Port 2:	[Enabled]	
	[2F8]	
Interrupt:	[IRQ3]	

```
F1  Help    ⇅ Select Item    -/+ Change Values        F9  Setup Defaults
ESC Exit    ↔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use the legend keys to make your selections and exit to the Main Menu.

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Use the following chart to configure the Input/Output settings: Keyboard Features Menu:

Table 5-9: I/O Device Configuration Options

FEATURE	OPTIONS	DESCRIPTION
Local Bus IDE Adapter	Disabled Primary Secondary Both	Enables the integrated local bus IDE adapter
USB Controller 3	Disabled Enabled	Enables/Disables one rear USB connector. (On customized boards there is also one front USB connector enabled/disabled.)
USB Controller 2 and 3	Disabled Enabled	Enables/Disables both rear USB connectors. (On customized boards there are also two front USB connectors enabled/disabled.)
USB Controller 1, 2 and 3	Disabled Enabled	Enables/Disables entire USB functionality. If disabled, all three USB connectors and the USB 2.0 controller are disabled.
USB EHCI Host Controller	Disabled Enabled	Controls USB 2.0 functionalitythrough this setup item
Legacy USB Support	Disabled Enabled	Enable support for legacy universal serial bus
Onboard LAN Controller	Disabled Enabled	Enables/Disables the ICH4 internal LAN controller. Setting this item to Disable will remove the LAN from the PCI Configuration Space
COM Port 1	Disabled Enabled	Enabled requires you to enter the base Input/Output address and the interrupt number of the SIO Com Ports.
COM Port 2	Disabled Enabled	Enabled requires you to enter the bas input/output address and the interrupt number of the SIO Com Ports.

Use this menu to specify how the I/O (Input and Output) ports are configured:

- Manually by you.
- Automatically by the BIOS during Post

Warning!

If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings. It also displays this message at the bottom of the menu:

* Indicates a DMA, Interrupt, I/O, or memory resource conflict with another device.

Resolve the conflict by selecting another settings for the devices.

5.2.5 Keyboard Features

Figure 5-9: Keyboard Features Menu - Screen Display

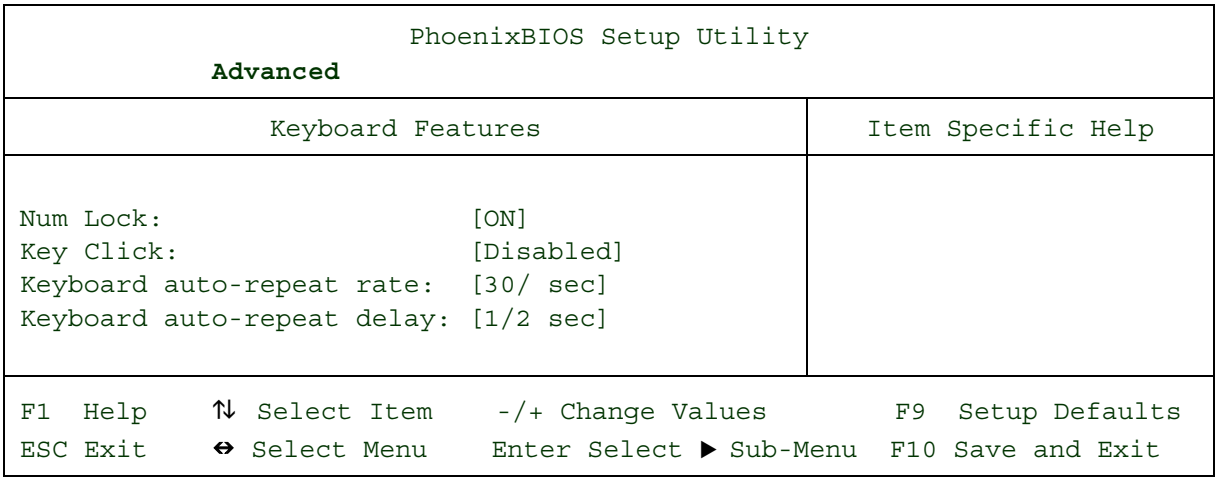

Table 5-10: Keyboard Features Options

FEATURE	OPTIONS	DESCRIPTION
Num Lock	AUTO ON OFF	Selects Power-on state for NumLock
Key Click	Disabled Enabled	Turns audible Key Click on
Keyboard auto-repeat rate	30/ sec 26.7/ sec 21.8/ sec 18.5/ sec 13.3/ sec 10/ sec 6/ sec 2/ sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	1/4 sec 1/2 sec 3/4 sec 1 sec	Set the delay time after the key is held down before it begins to repeat the keystroke.

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5.2.6 Miscellaneous

Figure 5-10: Miscellaneous Menu - Screen Display

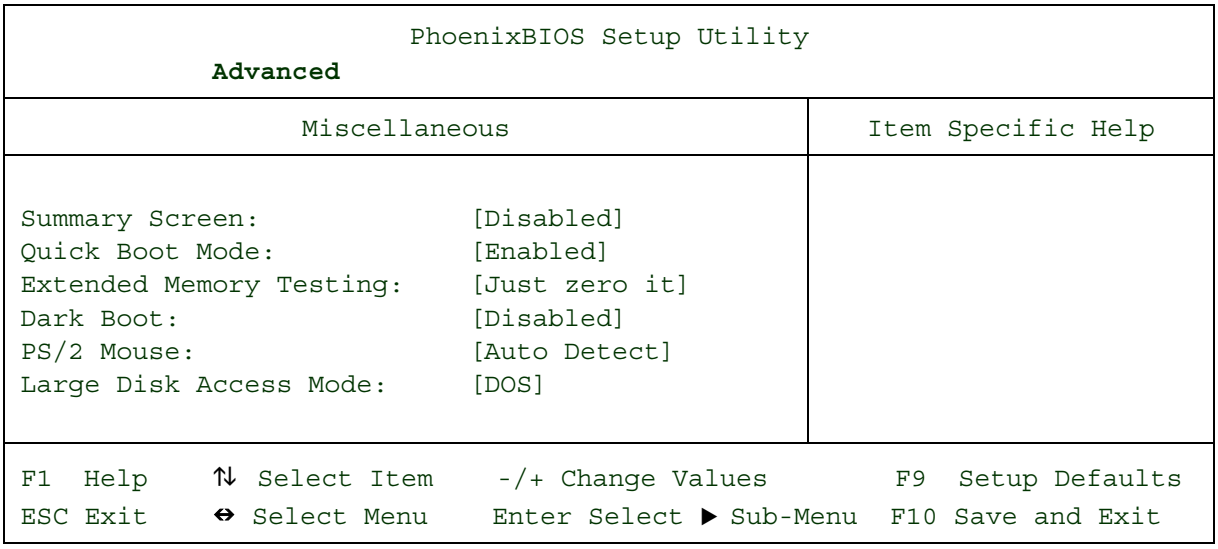

Table 5-11: Miscellaneous Options

FEATURE	OPTIONS	DESCRIPTION
Summary Screen	Disabled Enabled	Displays system configuration on boot.
Quick Boot Mode	Disabled Enabled	Allows the system to skip certain tests while booting. this will decrease the time needed to boot the system.
Extended Memory Testing	Just zero it None	Determines which type of test will be performed on extended memory (above 1 MB).
Dark Boot	Enabled Disabled	Prevents diagnostic screen output during boot.
PS/2 Mouse	Disabled Enabled Auto Detect	Disabled prevents any installed PS/2 mouse from functioning. Enabled forces PS/2 mouse to be enabled regardless if a mouse is present.
Large Disk Access Mode	Other DOS	Select DOS if you have DOS. Select Other if you have another OS such as Unix. A Large Disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.

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5.3 The Security Menu

Selecting "Security" from the menu bar displays a menu like this:

Figure 5-11: Security Menu - Screen Display

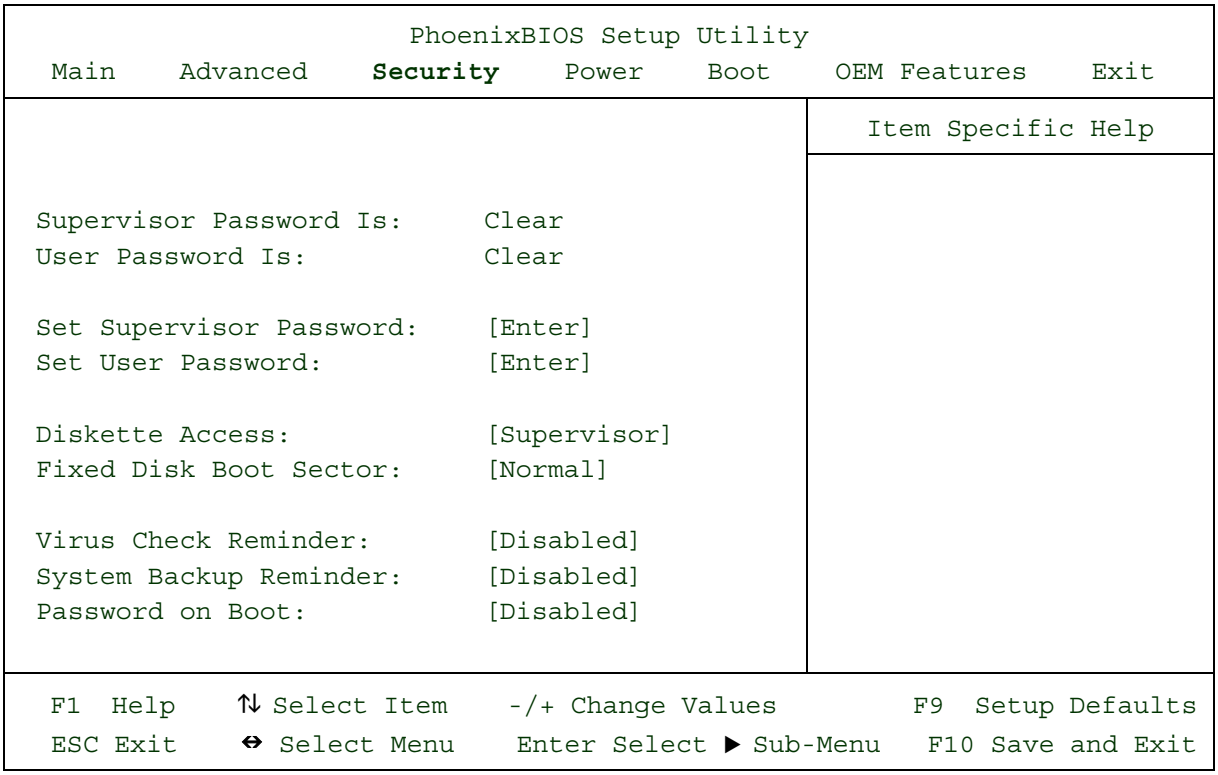

Table 5-12: Security Menu Options

FEATURE	OPTIONS	DESCRIPTION
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the password.
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the password.
Diskette Access	User Supervisor	Controls access to the diskette drives.
Fixed Diskboot Sector	Normal Write Protect	Write protects the boot sector on the hard disk to protect against viruses.
Virus Check Reminder System Backup Reminder	Disabled Daily Weekly Monthly	Displays the reminder message at boot.
Password on boot	Disabled Enabled	Enabled requires a password on boot, which requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.

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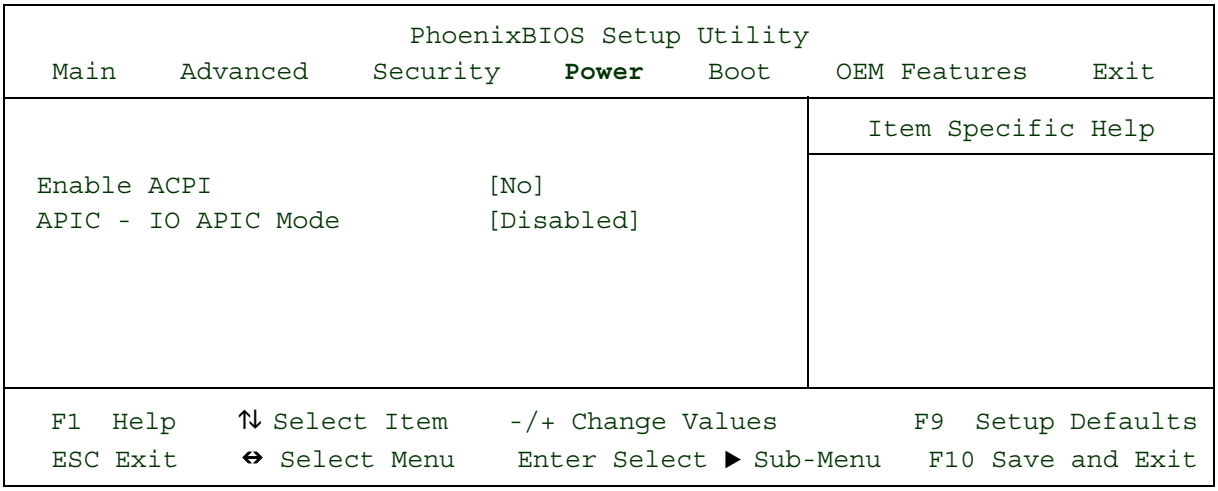
5.4 The Power Menu

Selecting "Power" from the menu bar displays a menu like this:

Figure 5-12: Power Menu - Screen Display



Use this menu to specify your settings for Power Management. Remember that the options available depend upon the hardware installed in your system. Those shown here are from a typical system.

A fresh installation of the OS must occur when activating the Power Management functions.

Use the legend keys to make your selections and exit to the Main Menu. Use the following chart in making your selections:

Table 5-13: Power Menu Options

FEATURE	OPTIONS	DESCRIPTION
Enable ACPI	No Yes	Enables/Disables ACPI BIOS (Advanced Configuration and Power Interface).
APIC - IO APIC Mode	Disabled Enabled	This item is valid only for Windows 2000 and Windows XP. A fresh installation of the OS must also occur when the APIC Mode is desired.

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5.5 Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as Windows 2000) from the device of your choice. If it cannot find the operating system on that device, it will attempt to load it from one or more other devices in the order specified in the Boot Menu. Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g., Iomega Zip drives), and network cards.

Note ...

Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device. Most PCs come with an operating system already installed on hard-drive C.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Figure 5-13: Boot Menu - Screen Display

```
                    PhoenixBIOS Setup Utility
Main   Advanced   Security   Power   Boot   OEM Features   Exit

                                              Item Specific Help

Boot Priority Order:                          Keys used to view or
1: USB Key:                                   configure devices:
2: IDE CD:                                    <+> or <-> moves the
3: IDE 0:                                     device up or down.
4: IDE 2:                                     <f> or <r> specifies
5:                                            the device fixed or
6:                                            removable.
7:                                            <x> excludes or
8:                                            includes the device to
                                              boot.
                                              <Shift+1> enables or
Excluded from Boot Order:                     disables a device.
:  IDE1:                                      <1-4> loads the default
:  IDE3:                                      boot sequence
:  USB FDC:
:  USB HDD:
:  USB CD-ROM:
:  USB ZIP:
:  USB LS120:
:  PCI BEV:
:  PCI SCSI:
:  Bootable Add-In Cards

F1  Help   ↑↓ Select Item   -/+ Change Values     F9  Setup Defaults
ESC Exit   ↔ Select Menu    Enter Select ▶ Sub-Menu   F10 Save and Exit
```

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This BIOS includes a feature for booting from LAN using the BOOTP / DHCP protocol.

Lan-Boot is based on Etherboot 5.2.5, a LAN-Boot implementation, which is covered by the GNU public license. It has been adopted for use with Kontron CompactPCI Hardware. As required by the GNU public license, the complete source code and further information are available via the internet (www.sourceforge.net).

Using this option requires an understanding of the BOOTP and/or DHCP mechanisms and knowledge in configuring a BOOTP or DHCP server. These topics are not described within this-manual.

Note ...

Floppy drives are not managed on this menu as part of Removable Devices.

To change a device's priority on the list, first select it with the up-or-down arrows, and move it up or down using the <+> and <-> keys. Pressing <x> includes or excludes a device in the boot priority order list.

This menu allows selecting the order of the devices from which the BIOS attempts to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one on the list.

The Boot Menu shows two lists, the boot priority list and the exclude from boot order list.

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5.6 OEM Features Menu

Selecting "OEM Features" from the menu bar displays a menu like this:

Figure 5-14: OEM Features Menu - Screen Display

```
                    PhoenixBIOS Setup Utility
 Main    Advanced    Security    Power    Boot    OEM Features    Exit

                                                   Item Specific Help

▶ PC Health
▶ Watchdog Settings
▶ Temperature Management
▶ Front-Rear I/O
▶ System Info

SpeedStep                          [Step0]
Spread Spectrum Modulation         [Disabled]
Reset PCI-to-PCI bridges           [Disabled]
Delay after P2P Reset              [Disabled]
Delay for PCI Config Cycle         [Disabled]
Accept CL.FFh for PCI-Dev          [YES]
Power-On Delay for USB Devices     [Disabled]
Onboard lan RPL ROM                [Disabled]
Load JRC BIOS Extension            [YES]
Serialized IRQ for Cardbus         [Disabled]

 F1  Help   ↑↓ Select Item   -/+ Change Values      F9  Setup Defaults
 ESC Exit   ↔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use the legend keys to make your selections and exit to the Main Menu. Use the following chart in making your selections:

Table 5-14: OEM Features Options

FEATURE	OPTIONS	DESCRIPTION
SpeedStep	Step0 - Step7	This item is to reduce the CPU speed. See the table 5-15 to find out which step belongs to which speed.
Spread Spectrum Modulation	Disabled 0.5%	Enable clock spreading. Spread spectrum typically reduces system EMI.
Reset PCI-to-PCI Bridges	Disabled Enabled	The BIOS may reset the PCI-to-PCI bridges in the system using a software reset mechanism. Especially when the board is used in conjunction with hot swap compatible boards elsewhere in the system, it should be disabled. Default is disabled.
Delay after P2P Reset	Disabled 1 ms 5 ms 10 ms	Select delay after PCI-to-PCI reset.
Delay f.PCI Config Cycle	Disabled 100ms; 200ms; 300ms; 500ms; 800ms	Delay time for PCI config cycles for all devices
Accept Cl.FFh for PCI-Dev	Yes No	Some PCI boards use the class code 0FFh. Boards with class code FF are distributed by some vendors in the knowledge that there will be different handling of such devices. The PCI standard does not define configuration rules for class code FF. By setting this field to “Yes”, these non-standard boards will also be configured by the BIOS and made operable.
Power-On Delay for USB Devices	Disabled 5s	This additional delay time fixes sporadic non-function on some specific USB devices. This increases boot time by seconds. Normally this should be switched to Disabled.
Onboard LAN RPL ROM	Disabled Fast Ethernet	Enable LAN BOOT
Load JRC BIOS Extension	Yes No	For saving space in the ROM area. Select No: JRC extension will not be loaded.
Serialized IRQ for Cardbus	Disabled Enabled	Enables/disables special handling of the Texas Instruments Cardbus controller PCI1420.

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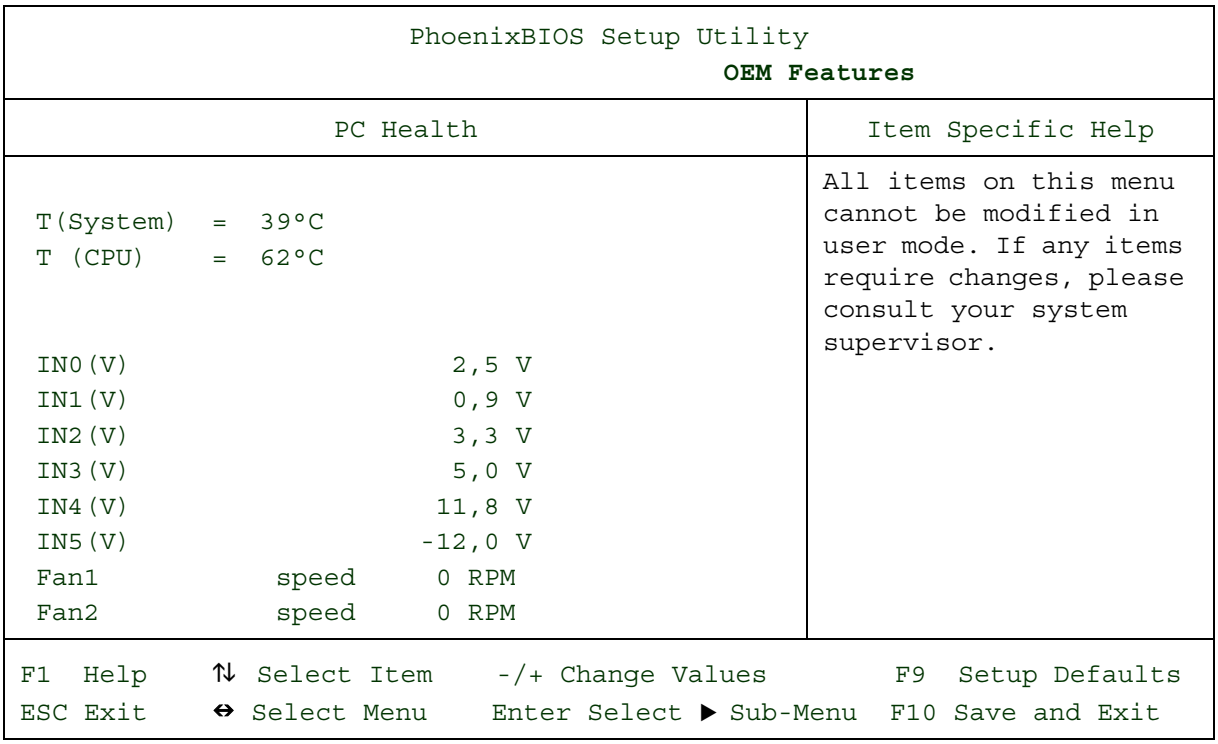
Table 5-15: SpeedStep Frequency Table

Frequency	1.1 GHz	1.6 GHz	1.8 GHz
1.8 GHz			Step0
1.6 GHz		Step0	Step1
1.4 GHz		Step1	Step2
1.3 GHz			
1.2 GHz		Step2	Step3
1.1 GHz	Step0		
1.0 GHz	Step1	Step3	
900 MHz	Step2		
800 MHz	Step3	Step4	Step4
600 MHz	Step4, Step5, Step6, Step7	Step5, Step6, Step7	Step5, Step6, Step7

5.6.1 PC Health

Figure 5-15: PC Health - Screen Display



5.6.2 Watchdog Settings

Figure 5-16: Watchdog Settings - Screen Display

```
PhoenixBIOS Setup Utility
                                        OEM Features

Watchdog Settings                       | Item Specific Help

    IRQ5 Routing                [Disabled]
    Watchdog Mode               [Disabled]
    WDT Active Time             [2s]
    Active for boot             [Disabled]
    Fail signal                 [Disabled]
    Resource 280h

F1  Help   ↑↓ Select Item   -/+ Change Values     F9  Setup Defaults
ESC Exit   ↔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Table 5-16: Watchdog Settings Options

FEATURE	OPTIONS	DESCRIPTION
IRQ5 routing	Disabled Watchdog Derate Signal Enum Signal Fail Signal	Reserve resource 280h and IRQ5 for watchdog, derate, Enum or Fail signal. Fail signal from the power supply. Enum signal is generated by a hot swap compatible board after insertion and prior to removal. Derate signal indicates that the power supply is beginning to derate its power output.
Watchdog mode	Disabled NMI Reset Cascade (NMI + Reset)	Watchdog routing to NMI, NMI + Reset or Reset
WDT Active Time	125ms, 250 ms, 500ms, 1s, 2s, 4s, 8s, 16s, 32s, 64s, 128s, 256s	Select the time after which the action selected occurs, if the watchdog timer is not retriggered.
Active for boot	Disabled Enabled	Select Enable if the watchdog timer requires to be started before the operating system is booted from the BIOS.
Fail Signal	Disabled NMI	Fail signal from the power supply. If this signal is to used inside an application, it may be routed to NMI here.

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5.6.3 Temperature Management

Figure 5-17: Temperature Management - Screen Display

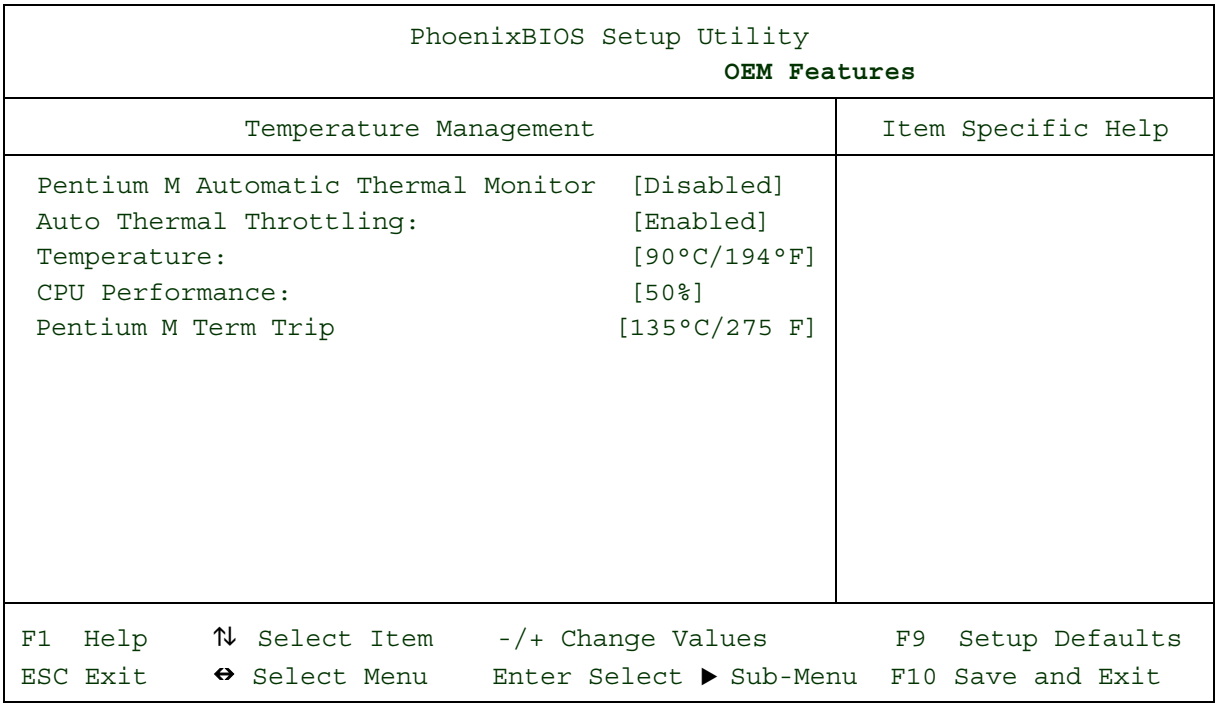

Table 5-17: Temperature Management Options

FEATURE	OPTIONS	DESCRIPTION
Pentium M Automatic Thermal Monitor	Disabled Enabled	Thermal Monitor is enabled and when the die temperature is very near to the temperature limits of the processor, the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor.
Auto Thermal Throttling	Enabled Disabled	Reduces CPU speed to avoid overheating
Temperature	95°C – 110°C	CPU clock throttling starts when select Temperature is reached.
CPU Performance	12.5% 25% 50% 75%	The CPU performance will be reduced to the selected value when reaching the temperature threshold.
Pentium M Term Trip	N/A	Shows the Pentium M max Temperature

5.6.4 Front-Rear I/O

Figure 5-18: Front-Rear I/O - Screen Display

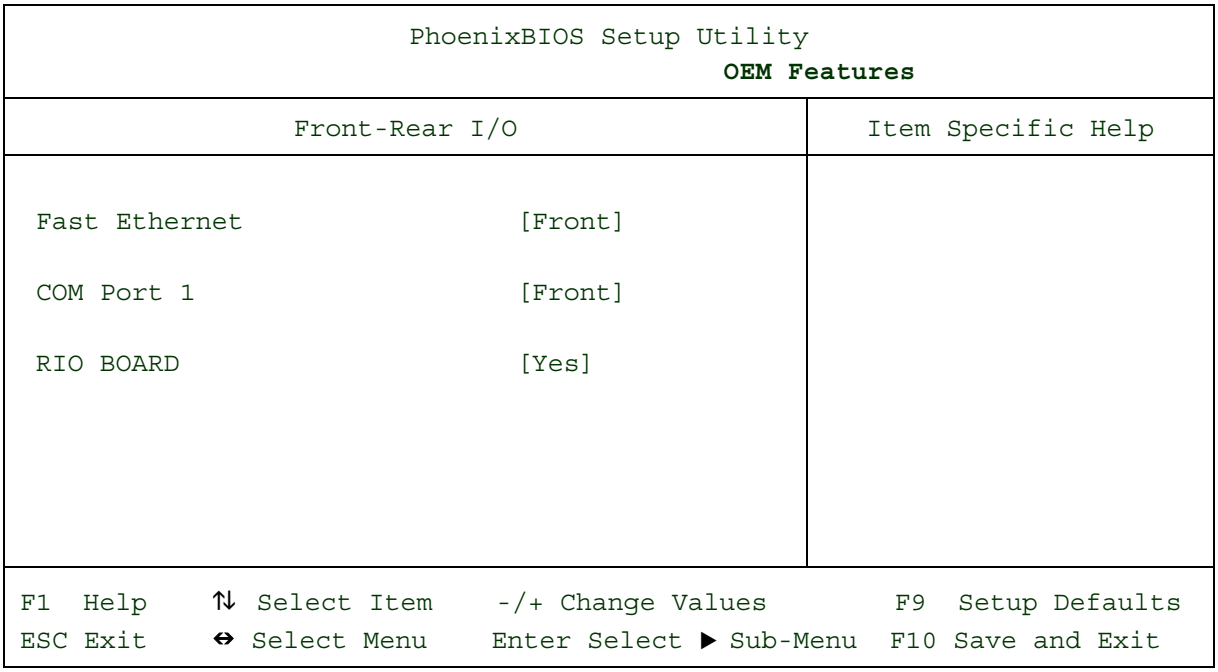

Table 5-18: Front-Rear I/O Options

FEATURE	OPTIONS	DESCRIPTION
Fast Ethernet	Front Rear Auto	Configure Fast Ethernet port either for physical connection to the Front Panel or to the Rear I/O connector (back).
COM Port 1	Front Rear	Configure COM Port 1 either for physical connection to the Front Panel or to the Rear I/O connector (back).
RIO BOARD	N/A	This is a display only field, which indicates whether the board is Rear I/O configured.

5.6.5 System Info

Figure 5-19: System Info - Screen Display

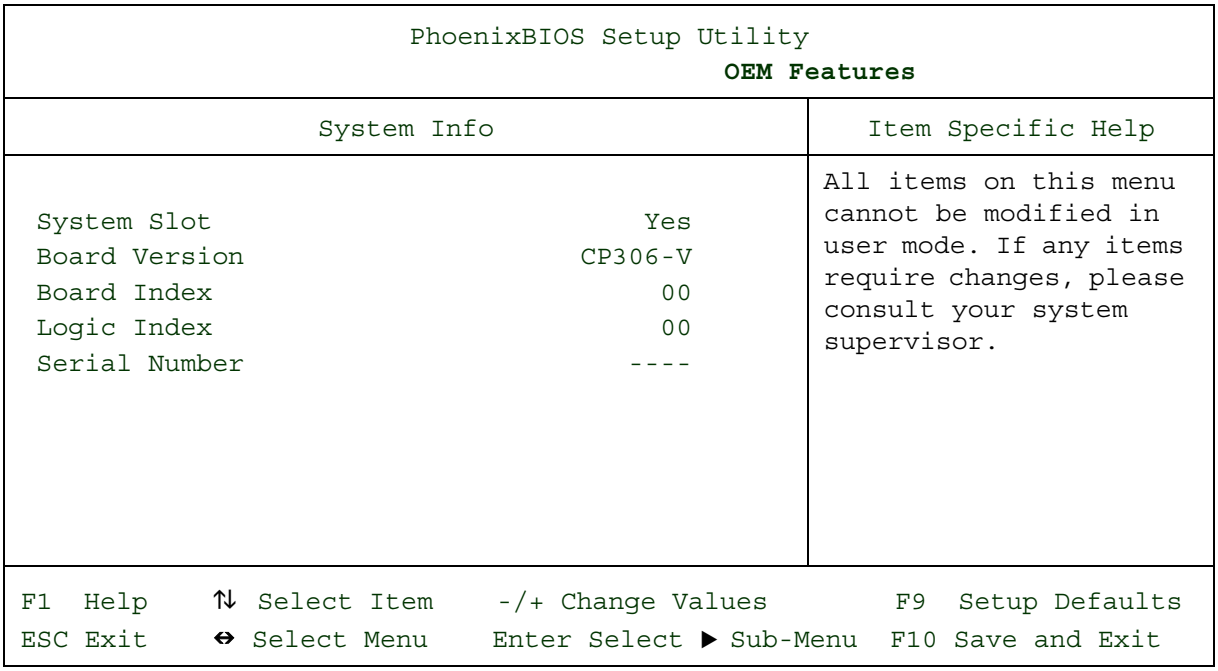

Table 5-19: System Info Options

FEATURE	OPTIONS	DESCRIPTION
System Slot	Yes No	Displays whether the board is in a system slot or not.
Board Version	N/A	This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.
Board Index	N/A	This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.
Logic Index	N/A	This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic.
Serial Number	N/A	This is a display only field. The serial number is unique to each board produced by Kontron. It could be used also by the customer to identify specific boards.

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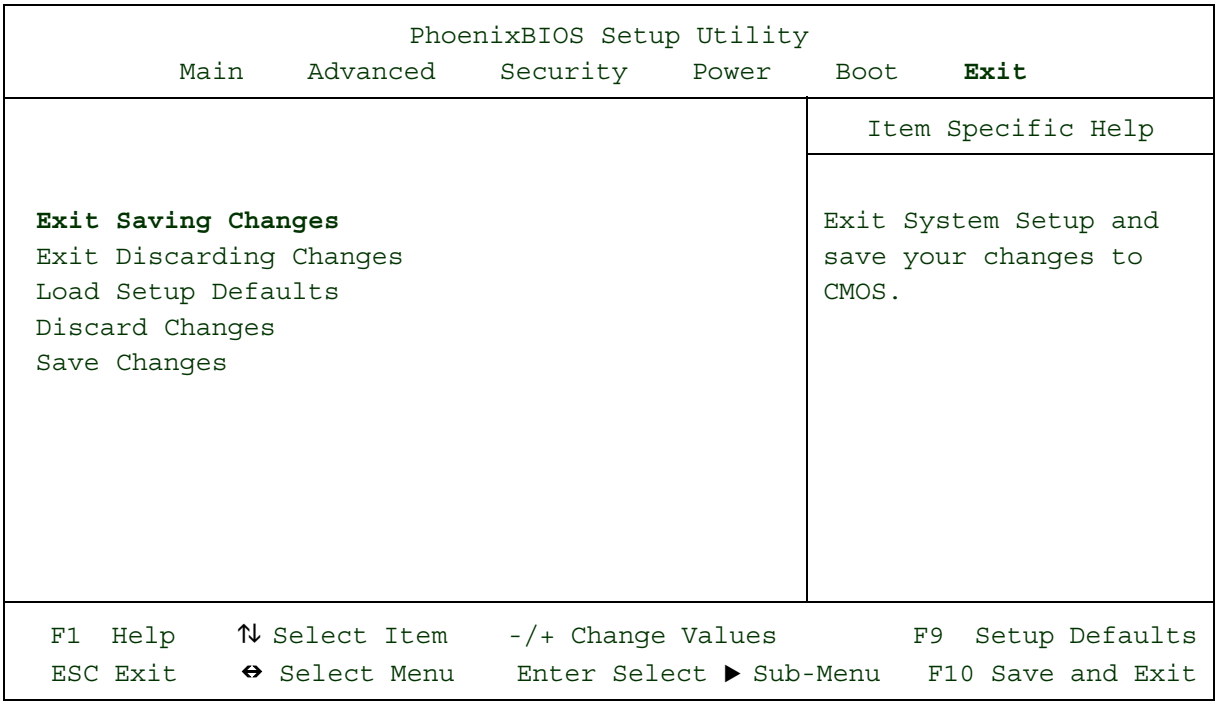
5.7 The Exit Menu

Selecting "Exit" from the menu bar displays this menu:

Figure 5-20: Exit Menu - Screen Display



The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit

5.7.1 Saving Values

After making your selections on the Setup menus, always select either "Exit Saving Changes" or "Save Changes." Both procedures store the selections displayed in the menus in **CMOS** (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

If you attempt to exit without saving, the program asks if you want to save before exiting.

During boot up, *Phoenix*BIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press **<F2>** to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

5.7.2 Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

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5.7.3 Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu. The program displays this message

If, during boot up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP

Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press **<F1>** to resume the boot or **<F2>** to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

5.7.4 Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS

Selecting “Discard Changes” on the Exit menu updates all the selections and displays this message:

5.7.5 Save Changes

Selecting “Save Changes” saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

5.8 PhoenixBIOS Messages

The following is a list of the messages that the BIOS can display. Most of them occur during POST. Some of them display information about a hardware device, e.g., the amount of memory installed. Others may indicate a problem with a device, such as the way it has been configured. Following the list are explanations of the messages and remedies for reported problems.

* If your system displays one of the messages marked below with an asterisk (*), write down the message and contact your dealer. If your system fails after you make changes in the Setup menus, reset the computer, enter Setup and install Setup defaults or correct the error.

0200 Failure Fixed Disk

Fixed disk is not working or not configured properly. Check to see if fixed disk is attached properly. Run Setup. Find out if the fixed-disk type is correctly identified.

0210 Stuck key

Stuck key on keyboard.

0211 Keyboard error

Keyboard not working.

***0212 Keyboard Controller Failed**

Keyboard controller failed test. May require replacing keyboard controller.

0213 Keyboard locked - Unlock key switch

Unlock the system to proceed.

0220 Monitor type does not match CMOS - Run SETUP

Monitor type not correctly identified in Setup

***0230 Shadow Ram Failed at offset: nnnn**

Shadow RAM failed at offset: <nnnn> of the 64k block at which the error was detected.

***0231 System RAM Failed at offset: nnnn**

System RAM failed at offset: <nnnn> of in the 64k block at which the error was detected.

***0232 Extended RAM Failed at offset: nnnn**

Extended memory not working or not configured properly at offset: <nnnn>.

0250 System battery is dead - Replace and run SETUP

The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.

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0251 System CMOS checksum bad - Default configuration used

System CMOS has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. The BIOS installed Default Setup Values. If you do not want these values, enter Setup and enter your own values. If the error persists, check the system battery or contact your dealer.

*0260 System timer error

The timer test failed. Requires repair of system board.

*0270 Real time clock error

Real-Time Clock fails BIOS hardware test. May require board repair.

0271 Check date and time settings

BIOS found date or time out of range and reset the Real-Time Clock. May require setting legal date (1991-2099).

0280 Previous boot incomplete - Default configuration used

Previous POST did not complete successfully. POST loads default values and offers to run Set-up. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail. On systems with control of **wait states**, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error is cleared the next time the system is booted.

0281 Memory Size found by POST differed from CMOS

Memory size found by POST differed from CMOS.

02B0 Diskette drive A error

02B1 Diskette drive B error

Drive A: or B: is present but fails the BIOS POST diskette tests. Check to see that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.

02B2 Incorrect Drive A type - run SETUP

Type of floppy drive A: not correctly identified in Setup.

02B3 Incorrect Drive B type - run SETUP

Type of floppy drive B: not correctly identified in Setup.

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02D0 System cache error - Cache disabled

RAM cache failed and BIOS disabled the cache. On older boards, check the cache jumpers. You may have to replace the cache. See your dealer. A disabled cache slows system performance considerably.

02F0: CPU ID:

CPU socket number for Multi-Processor error.

***02F4: EISA CMOS not writeable**

ServerBIOS2 test error: Cannot write to EISA CMOS.

***02F5: DMA Test Failed**

ServerBIOS2 test error: Cannot write to extended **DMA** (Direct Memory Access) registers.

***02F6: Software NMI Failed**

ServerBIOS2 test error: Cannot generate software NMI (Non-Maskable Interrupt).

***02F7: Fail-Safe Timer NMI Failed**

ServerBIOS2 test error: Fail-Safe Timer takes too long.

device Address Conflict

Address conflict for specified: <device>

`Allocation Error for:` <device>

Run ISA or EISA Configuration Utility to resolve resource conflict for the specified: <device>

CD ROM Drive

CD ROM Drive identified.

Entering SETUP ...

Starting Setup program

***Failing Bits: nnnn**

The hex number: <nnnn> is a map of the bits at the RAM address which failed the memory test. Each 1 (one) in the map indicates a failed bit. See errors 230, 231, or 232 above for offset address of the failure in System, Extended, or Shadow memory.

Fixed Disk n

Fixed disk n (0-3) identified.

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Invalid System Configuration Data

Problem with NVRAM (CMOS) data.

I/O device IRQ conflict

I/O device IRQ conflict error.

PS/2 Mouse Boot Summary Screen:

PS/2 Mouse installed.

nnnn kB Extended RAM Passed

Where: <nnnn> is the amount of RAM in kilobytes successfully tested.

nnnn Cache SRAM Passed

Where: <nnnn> is the amount of system cache in kilobytes successfully tested.

nnnn kB Shadow RAM Passed

Where: <nnnn> is the amount of shadow RAM in kilobytes successfully tested.

nnnn kB System RAM Passed

Where: <nnnn> is the amount of system RAM in kilobytes successfully tested.

One or more I2O Block Storage Devices were excluded from the Setup Boot Menu

There was not enough room in the IPL table to display all installed I2O block-storage devices.

Operating system not found

Operating system cannot be located on either drive A: or drive C:. Enter Setup and see if fixed disk and drive A: are properly identified.

***Parity Check 1 nnnn**

Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays: ????. Parity is a method for checking errors in binary data. A parity error indicates that some data has been corrupted.

***Parity Check 2 nnnn**

Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.

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Press <F1> to resume, <F2> to Setup, <F3> for previous

Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change the settings. Press <F3> to display the previous screen (usually an initialization error of an **Option ROM**, i.e., an add-on card). Write down and follow the information shown on the screen.

Press <F2> to enter Setup

Optional message displayed during POST. Can be turned off in Setup.

PS/2 Mouse

PS/2 mouse identified.

Run the I2O Configuration Utility

One or more unclaimed block storage devices have the Configuration Request bit set in the LCT. Run an I2O Configuration Utility (e.g. the SAC utility).

System BIOS shadowed

System BIOS copied to shadow RAM.

UMB upper limit segment address: <nnnn>

Displays the address: <nnnn> of the upper limit of **Upper Memory Blocks**, indicating released segments of the BIOS which can be reclaimed by a virtual memory manager.

Video BIOS shadowed

Video BIOS successfully copied to shadow RAM.

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5.9 Phoenix Phlash16

Phoenix Phlash16 gives you the ability to update your BIOS from a floppy disk without having to install a new ROM BIOS chip.

Phoenix Phlash16 is a utility for "flashing" (copying) a BIOS to the Flash memory installed on your computer from a floppy disk. A Flash memory is a chip that you can write to using a special method called "flashing." Use Phoenix Phlash16 for updating the current BIOS with a new version.

5.9.1 Installation

Phoenix Phlash16 is shipped with your computer as a compressed file called CRISDISK.ZIP that contains the following files:

CRISDISK.BAT	Executable file for creating the Crisis Recovery Diskette.
PHLASH16.EXE	Programs the flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.WPH	Actual BIOS image to be programmed into flash ROM.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.

5.9.2 Executing Phoenix Phlash16

Phoenix Phlash is operated in the Command Line mode.

Warning!

For your own protection, be sure you have a Crisis Recovery Diskette ready to use before executing Phlash.

5.9.2.1 Command Line Mode

Use this mode to update or replace your current BIOS. To execute Phlash in this mode, move to the directory into which you have installed Phoenix Phlash and type the following:

phlash16

Phoenix Phlash16 will automatically update or replace the current BIOS with the one which your OEM or dealer supplies you.

Phlash16 may fail if your system is using memory managers, in which case the utility displays the following message:

Cannot flash when memory managers are present.

If you see this message after you execute Phlash16, you must disable the memory manager on your system. To do so, follow the instructions in the following sections.

Disabling Memory Managers

To avoid failure when flashing, you must disable the memory managers that load from CONFIG.SYS and AUTOEXEC.BAT. There are two recommended procedures for disabling the memory managers. One consists of pressing the <F5> key (only if you are using DOS 5.0 or above), and the other requires the creation of a boot diskette.

DOS 5.0 (or later version)

For DOS 5.0 and later, follow the two steps below to disable any memory managers on your system. If you are not using at least DOS 5.0, then you must create a boot diskette to bypass any memory managers (See Create a Boot Diskette, below).

1. Boot DOS 5.0 or later version. (In Windows 95, at the boot option screen, choose Option 8, "Boot to a previous version of DOS.")
2. When DOS displays the “Starting MS-DOS” message, press <F5>.

After you press <F5>, DOS bypasses the CONFIG.SYS and AUTOEXEC.BAT files, and therefore does not load any memory managers.

You can now execute Phlash16.

Create a Boot Diskette

To bypass memory managers in DOS versions previous to 5.0, follow this recommended procedure:

1. Insert a diskette into your A: drive.
2. Enter the following from the command line:

   Format A: /S

3. Reboot your system from the A: drive.

Your system will now boot without loading the memory managers, and you can then execute Phlash16.

5.9.3 JRC JUMP*tec*® Remote Control

The JUMP*tec* Remote Control (JRC) is an extension of the PC BIOS that provides a way to intercept and reroute certain BIOS functionality over a serial port at an early stage during the system’s boot process.

Requirements:

- Regular PC (host PC) running either
  - Windows 9x or Windows NT with jrc.exe installed
  - MS-DOS with jrcd.exe installed
- Serial cable that connects either of the two PC com ports

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Table 5-20: COM Ports Pinout

X_1			X_2
SIGNAL	PIN	PIN	SIGNAL
Receive data	2	3	Transmit data
Transmit data	3	2	Receive data
GND	5	5	GND

Operating Instructions:

- Open a command prompt window on the host PC when running Windows 9x or Windows NT
- Issue a connect command with the appropriate COM port and the desired baud rate.

  jrc server.<com port><max baud rate>
- you can exit the server mode by pressing both control keys on the keyboard simultaneously.

5.10 POST Errors and Beep Codes

5.10.1 Recoverable POST Errors

Whenever a recoverable error occurs during POST, *Phoenix*BIOS displays an error message describing the problem.

*Phoenix*BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (e.g. VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

5.10.2 Terminal POST Errors

There are several POST routines that issue a **POST Terminal Error** and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters).

The routine derives the beep code from the test point error as follows:

1. The 8-bit error code is broken down to four 2-bit groups (Discard the most significant group if it is 00).
2. Each group is made one-based (1 through 4) by adding.
3. Short beeps are generated for the number in each group. Example:

Test point 01Ah = 00 01 10 10 = 1-2-3-3 beeps

5.10.3 Test Points and Beep Codes

At the beginning of each POST routine, the BIOS outputs the test point error code to I/O address 80h. Use this code during trouble shooting to establish at what point the system failed and what routine was being performed.

Some motherboards are equipped with a seven-segment LED display that displays the current value of port 80h. For production boards that do not contain the LED display, you can purchase a card that performs the same function. If the BIOS detects a terminal error condition, it halts POST after issuing a terminal error beep code (See above) and attempting to display the error code on upper left corner of the screen and on the port 80h LED display. It attempts repeatedly to write the error to the screen. This may cause "hash" on some CGA displays. If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

The following is a list of the checkpoint codes written at the start of each test and the beep codes issued for terminal errors. Unless otherwise noted, these codes are valid for Phoenix-BIOS 4.0 Release 6.x.

Table 5-21: Checkpoint and Beep Codes

CODE	BEEPS	POST ROUTINE DESCRIPTION
02h		Verify Real Mode
03h		Disable Non-Maskable Interrupt (NMI)
04h		Get CPU type
06h		Initialize system hardware
07h		Disable shadow and execute code from the ROM
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize the local bus IDE
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Auto size
18h		8254 timer initialization
1Ah		8237 DMA controller initialization

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Table 5-21: Checkpoint and Beep Codes (cont'd)

CODE	BEEPS	POST ROUTINE DESCRIPTION
1Ch		Reset Programmable Interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
28h		Auto size DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 kB base RAM
2Ch	1-3-4-1	RAM failure on address line ***xxxx****
2Eh	1-3-4-3	RAM failure on data bits ***xxxx**** of low byte of memory bus
2Fh		Enable cache before system BIOS shadow
32h		Test CPU bus-clock frequency
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Auto size cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
41h		Initialize extended memory for RomPilot
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
47h		Initialize I20 support
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Initialize MultiBoot
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled

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Table 5-21: Checkpoint and Beep Codes (cont'd)

CODE	BEEPS	POST ROUTINE DESCRIPTION
55h		Enable USB devices
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Disable CPU cache
5Ch		Test RAM between 512 and 640 kB
60h		Test extended memory
62h		Test extended memory address lines
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		Initialize Multi Processor APIC
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display shadow-area message
6Eh		Display possible high address for UMB recovery
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		Initialize Intelligent System Monitoring
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialization
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports
87h		Configure Motherboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area

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Table 5-21: Checkpoint and Beep Codes (cont'd)

CODE	BEEPS	POST ROUTINE DESCRIPTION
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Initialize local-bus hard-disk controllers
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register (optional)
97h		Fix up Multi Processor table
98h	1-2	Search for option ROMs One long, two short beeps on checksum failure
99h		Check for SMART Drive (optional)
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives
A0h		Set time of day
A2h		Check key lock
A4h		Initialize typematic rate
A8h		Erase F2 prompt
AAh		Scan for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B1h		Inform RomPilot about the end of POST
B2h		POST done - prepare to boot operating system
B4h	1	One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B7h		Initialize ACPI BIOS
B9h		Prepare Boot
BAh		Initialize SMBIOS

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Table 5-21: Checkpoint and Beep Codes (cont'd)

CODE	BEEPS	POST ROUTINE DESCRIPTION
BBh		Initialize PnP Option ROMs
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and backup reminders
C0h		Try to boot with INT 19
C1h		Initialize POST Error Manager (PEM)
C2h		Initialize error logging
C3h		Initialize error display function
C4h		Initialize system error handler
C5h		PnPnd dual CMOS (optional)
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
CAh		Redirect Int 15h to enable remote keyboard
CBh		Redirect Int 13h to Memory Technology Devices such as ROM, RAM, PCMCIA, and serial disk
CCh		Redirect Int 10h to enable remote serial video
CDh		Re-map I/O and memory for PCMCIA
CEh		Initialize digitizer and display message
D2h		Unknown interrupt
The following are for boot block in Flash ROM		
E0h		Initialize the chipset
E1h		Initialize the bridge
E2h		Initialize the CPU
E3h		Initialize system timer
E4h		Initialize system I/O
E5h		Check force recovery boot
E6h		Checksum BIOS ROM
E7h		Go to BIOS
E8h		Set Huge Segment
E9h		Initialize Multi Processor
EAh		Initialize OEM special code

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Table 5-21: Checkpoint and Beep Codes (cont'd)

CODE	BEEPS	POST ROUTINE DESCRIPTION
EBh		Initialize PIC and DMA
ECh		Initialize Memory type
EDh		Initialize Memory size
EEh		Shadow Boot Block
EFh		System memory test
F0h		Initialize interrupt vectors
F1h		Initialize Run Time Clock
F2h		Initialize video
F3h		Initialize System Management Manager
F4h		Output one beep
F5h		Clear Huge Segment
F6h		Boot to Mini DOS
F7h		Boot to Full DOS

* If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word-bitmap (xxxx) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80 LED display. It first displays the checkpoint code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

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Chapter 6

Power Considerations

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6. Power Considerations

6.1 System Power

Some processors of the new Intel Pentium M processor family require more power than earlier Pentium lll processors, but less than the Pentium 4. This results in special requirements for the power supply and the backplane. The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the CP306-V system environment.

6.2 CP306-V Voltage Ranges

The CP306-V board itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP306-V should be carefully tested to ensure compliance with these ratings.

Table 6-1: Absolute Maximum Ratings

SUPPLY VOLTAGE	ABSOLUTE MAXIMUM RATINGS
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP306-V is not guaranteed to function if the board is not operated within the prescribed limits.

Table 6-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE	REMARKS
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.	Main voltage
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.	Main voltage
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.	Not required
-12 V	-11.4 V min. to -12.6 V max.	-12 V min. to -12.6 V max.	Not required

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6.3 Backplane Requirements

Backplanes to be used with the CP306-V must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs. It is recommended to use only backplanes which have two power planes for the 3.3 V and +5 V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

6.4 Power Supply Units

Power supplies for the CP306-V must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP306-V has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP306-V is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP306-V may hangup. The solution is to use an industrial PSU or to add more load to the system.

If DC/DC power supplies are used, please ensure that the external main supply provides sufficient power in order to start-up the system properly. The external main supply should provide at least as much power as the system power supply is able to provide taking into consideration the inrush current.

Warning!

An underdimensioned power supply may cause damage to system components.

The start-up behavior of CompactPCI and PCI (ATX) power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply. The required behavior is described in the ATX (http://www.formfactors.org/FFDetail.asp?FFID=1&CatID=2) and the CompactPCI (PICMG, http://www.picmgeu.org/) specification.

6.4.1 Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the CP306-V.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

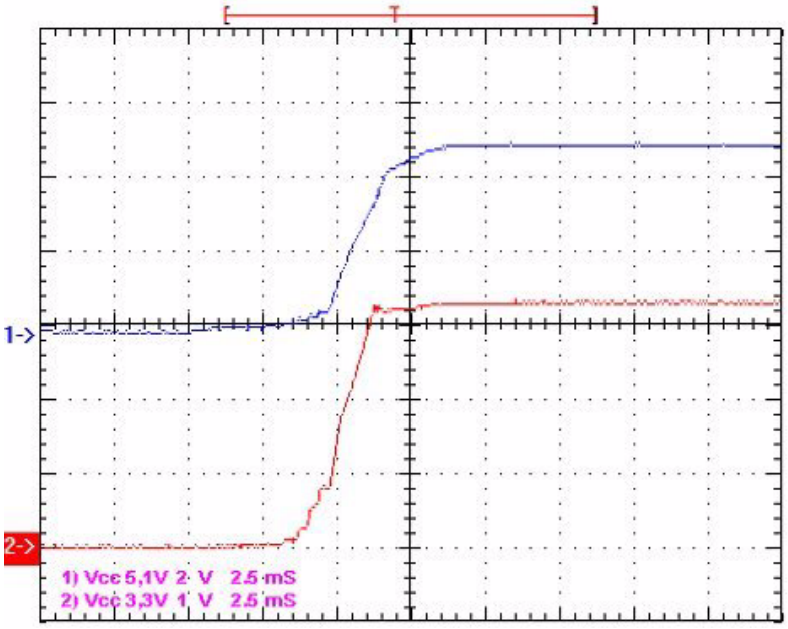
6.4.2 Voltage Sequencing Requirements

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

6.4.3 Rise Time Diagram

The following figure illustrates an example of the recommended voltage ramp of a CompactPCI power supply for all Kontron boards delivered up to now.

Figure 6-1: Voltage Ramp of the CP3-SVE180 AC Power Supply



6.4.4 Recommended Operating Conditions

The tolerance of the voltage lines is described in the CompactPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CompactPCI connector on the CPU board.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

The following table provides information regarding the required characteristics for each board input voltage.

Table 6-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)
5 V	+5.0 VDC	+5%/-3%	50 mV
3.3 V	+3.3 VDC	+5%/-3%	50 mV
+12 V	+12 VDC	+5%/-5%	240 mV
-12 V	-12 VDC	+5%/-5%	240 mV
V I/O (PCI signaling voltage)	+3.3 VDC or +5 VDC	+5%/-3%	50 mV
GND	Ground, not directly connected to protective earth (PE)		

6.4.5 Supply Voltage Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP306-V is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP306-V may hang up. The solution is to use an industrial PSU or to add more load to the system.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

6.5 Power Consumption of the CP306-V

The goal of this description is to provide a method to calculate the power consumption for the CP306-V board and for additional configurations. The Celeron M and Pentium M processors dissipate the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the CP306-V board using Celeron M and Pentium M processors with 256 MB memory. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies: one for the CPU, and the other for the hard disk. The operating systems used were DOS and Windows 2000. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity.

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6.5.1 Power Consumption Using Celeron M and Real Applications

The power consumption in DOS was measured with power management not active.

Table 6-4: Power Consumption DOS Celeron M

POWER	CELERON M 1.3 GHz / 512 kB L2 Cache
Core	1.366 V
5 V	6.95 W
3.3 V	7.19 W
Total	14.14 W

The Power Consumption in Windows 2000 IDLE Mode was measured at a VGA resolution of 1024X768.

Table 6-5: Power Consumption Win 2000 IDLE Mode Celeron M

POWER	CELERON M 1.3 GHz / 512 kB L2 Cache
Core	1.366 V
5 V	2.25 W
3.3 V	6.0 W
Total	8.25 W

The Power Consumption in Windows 2000 at 100% CPU Usage (Game: 3D-Pinball) was measured at a VGA resolution of 1024X768.

Table 6-6: Power Consumption Win 2000 100% CPU Usage Celeron M

POWER	CELERON M 1.3 GHz / 512 kB L2 Cache
Core	1.366 V
5 V	10.2 W
3.3 V	6.34 W
Total	16.54 W

The Power Consumption in Windows 2000 3D Mark Benchmark was measured at a VGA resolution of 1024X768 using a high performance VGA application.

Table 6-7: Power Consumption Win 2000 3D Mark Benchmark Celeron M

POWER	CELERON M 1.3 GHz / 512 kB L2 Cache
Core	1.366 V
5 V	11.0 W
3.3 V	9.6 W
Total	20.6 W

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6.5.2 Power Consumption Using Celeron M and Testing Application

The Power Consumption in Windows 2000 High Power Tool was measured at a VGA resolution of 1024X768 with the processor running at maximum power consumption (no real application).

Table 6-8: Power Consumption Win 2000 High Power Tool Celeron M

POWER	CELERON M 1.3 GHz / 512 kB L2 Cache
Core	1.366 V
5 V	17.0 W
3.3 V	6.1 W
Total	23.1 W

Note ...

The values in the above table are measured using the Intel High Power Tool. This tool serves only for checking the onboard power supplies and does not represent the power consumption of the CP306-V during normal operation.

In normal software applications this maximum power consumption level will never be reached.

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6.5.3 Power Consumption Using Pentium M and Real Applications

The power consumption in DOS was measured with power management not active.

Table 6-9: Power Consumption DOS Pentium M

POWER	PENTIUM M 600 MHz / 2MB L2 Cache	PENTIUM M 1.6 GHz / 1MB L2 Cache	PENTIUM M 1.8 GHz / 2MB L2 Cache
Core	1.036 V	1.472 V	1.318 V
5 V	4.4 W	12.8 W	12.8 W
3.3 V	6.9 W	7.2 W	7.2 W
Total	11.3 W	20.0 W	20.0 W

The Power Consumption in Windows 2000 IDLE Mode was measured at a VGA resolution of 1024X768.

Table 6-10: Power Consumption Win 2000 IDLE Mode Pentium M

POWER	PENTIUM M 600 MHz / 2MB L2 Cache	PENTIUM M 1.6 GHz / 1MB L2 Cache	PENTIUM M 1.8 GHz / 2MB L2 Cache
Core	1.036 V	1.472 V	1.318 V
5 V	4.0 W	6.1 W	8.4 W
3.3 V	5.0 W	6.0 W	5.0 W
Total	9.0 W	12.1 W	13.4 W

The Power Consumption in Windows 2000 at 100% CPU Usage (Game: 3D-Pinball) was measured at a VGA resolution of 1024X768.

Table 6-11: Power Consumption Win 2000 100% CPU Usage Pentium M

POWER	PENTIUM M 600 MHz / 2MB L2 Cache	PENTIUM M 1.6 GHz / 1MB L2 Cache	PENTIUM M 1.8 GHz / 2MB L2 Cache
Core	1.036 V	1.472 V	1.318 V
5 V	5.8 W	20.05 W	17.6 W
3.3 V	5.4 W	6.34 W	5.4 W
Total	11.2 W	26.39 W	23.0 W

The Power Consumption in Windows 2000 3D Mark Benchmark was measured at a VGA resolution of 1024X768 using a high performance VGA application.

Table 6-12: Power Consumption Win 2000 3D Mark Benchmark Pentium M

POWER	PENTIUM M 600 MHz / 2MB L2 Cache	PENTIUM M 1.6 GHz / 1MB L2 Cache	PENTIUM M 1.8 GHz / 2MB L2 Cache
Core	1.036 V	1.472 V	1.318 V
5 V	5.9 W	22.0 W	15.6 W
3.3 V	7.8 W	9.6 W	7.9 W
Total	13.7 W	31.6 W	23.5 W

6.5.4 Power Consumption Using Pentium M and Testing Application

The Power Consumption in Windows 2000 High Power Tool was measured at a VGA resolution of 1024X768 with the processor running at maximum power consumption (no real application).

Table 6-13: Power Consumption Win 2000 High Power Tool Pentium M

POWER	PENTIUM M 600 MHz / 2MB L2 Cache	PENTIUM M 1.6 GHz / 1MB L2 Cache	PENTIUM M 1.8 GHz / 2MB L2 Cache
Core	1.036 V	1.472 V	1.318 V
5 V	6.5 W	30.0 W	23.9 W
3.3 V	4.8 W	6.1 W	5.6 W
Total	11.3 W	36.1 W	29.5 W

Note ...

The values in the above table are measured using the Intel High Power Tool. This tool serves only for checking the onboard power supplies and does not represent the power consumption of the CP306-V during normal operation.

In normal software applications this maximum power consumption level will never be reached.

6.6 Power Consumption of CP306-V Accessories

The following table indicates the power consumption of the CP306-V accessories.

Table 6-14: Power Consumption Table for CP306-V Accessories

MODULE	POWER 5 V	POWER 3.3 V AVERAGE
Keyboard	100 mW	—
512 MB DDR333	—	1 W - 2 W
1 GB DDR266	—	2 W - 4 W
CompactFlash	—	100 mW - 300 mW
2.5” HDD	2.5 - 5 W	—
CP306-V-IOIDE	less than 1 mW (without HDD and CF)	100 mW
CP-RIO3-03 Rear I/O	100 mW	100 mW

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6.7 Start-Up Current of the CP306-V

The following tables indicate the start-up current of the CP306-V during the first 2-3 seconds after the power supply has been switched on. The power consumption of the CP306-V during operation is indicated in tables 6-4 to 6-7 and 6-9 to 6-12.

Table 6-15: Start-Up Current of the CP306-V with Pentium M Processors

POWER		PENTIUM M 600 MHz	PENTIUM M 1.6 GHz	PENTIUM M 1.8 GHz
5 V	peak	5.5 A	5.5 A	5.5 A
	average	0.5 A	0.5 A	0.5 A
3.3 V	peak	5.0 A	5.0 A	5.0 A
	average	2.5 A	2.5 A	2.5 A

Table 6-16: Start-Up Current of the CP306-V with Celeron M Processors

POWER		CELERON M 1.3 GHz
5 V	peak	5.8 A
	average	1.8 A
3.3 V	peak	5.5 A
	average	2.0 A

For further information on the start-up current, contact Kontron's Technical Support.

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Chapter 7

System Considerations

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7. System Considerations

7.1 Thermal Management

The thermal energy dissipation of the new generation of Intel Celeron M and Pentium M processors is less than that of Celeron 4 and Pentium 4 processors, however, certain application configurations of the CP306-V require active thermal energy dissipation. This requires new technology to ensure that the processor's die temperature is maintained within factory specifications. The following sections provide system integrators with the necessary information to satisfy thermal requirements when implementing CP306-V applications.

7.1.1 Passive Thermal Regulation

The thermal management architecture implemented on the CP306-V can be described as being three separate but related functions. The goal of all three functions is to protect the processor and reduce processor power consumption. Enabling the thermal control circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

The three thermal protection functions provided by the processor are:

1. CPU internal thermal monitor:

   This functions controls the processor temperature by modulating the processor core clocks.

2. External (LM87) thermal monitor:

   This functions controls via the processor Stopclock signal the power consumption. While asserted, it has the effect of stopping the clock to many internal elements of the processor.

3. Thermtrip:

   In the event of a catastrophic cooling failure, the processor will automatically shut down when the die temperature has reached approximately ~135 °C, this event is called Thermtrip.

7.1.1.1 CPU Internal Thermal Supervision

This function can be enabled and disabled in the BIOS, whereby the default value is: disabled. When the internal thermal control circuit has been enabled and a high temperature situation occurs, the internal clocks are modulated by alternately turning the clocks off and on with a duty cycle dependent on the processor type (typically 30-50%). This results in the processor power dissipation being reduced accordingly. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. The thermal control circuit is automatically deactivated when the temperature goes below the internal thermal supervision point. The internal temperature sensor is located near on the hottest area of the processor die. Each processor is individually calibrated during manufacturing to eliminate any potential manufacturing variations.

Note ...

The duty cycle and the internal thermal supervision point is factory configured and cannot be modified. For all Celeron M and Pentium M processors the internal thermal supervision point is 100 °C.

7.1.1.2 CPU External Thermal Supervision

This function can be enabled and disabled in the BIOS, whereby the default value is: disabled. There are two independent and isolated thermal sensors in the Celeron M and Pentium M processors. One is the on-die thermal diode. The other is the temperature sensor used for the Thermal Monitor and for Thermtrip. The measured temperature of both sensors can vary significantly, whereby the temperature of the external measured on-die sensors is always lower.

When the external thermal control circuit has been enabled and a high temperature situation occurs, the front panel “TH” LED will be switch on and the external Stopclock signal of the processor will be modulated by alternately turning the clocks off and on at a duty cycle specified in the BIOS (12.5% - 75%) and the processor power dissipation will be reduced.

The thermal control circuit does not automatically go inactive once the temperature goes below the selected thermal trip point. Explicit software action is necessary to switch back to normal mode.

Note ...

The duty cycle and the external thermal supervision point can be configured in the BIOS. Please ensure that the appropriate values are set for the respective environment.

7.1.1.3 CPU Emergency Thermal Supervision

This function can not be enabled and disabled in the BIOS. It is always enabled to ensure that the processor is protected in any event.

Assertion of “Thermtrip” (Thermal Trip) indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. Once activated, Thermtrip remains latched until the CP306-V undergoes a cold restart is performed (all power off and then on again).

Note ...

Upon assertion of “Thermtrip”, the front panel overtemperature TH/GP LED flashes at regular intervals.

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7.1.1.4 Thermal Management Recommendations

If the CP306-V is operated in a properly configured CompactPCI environment with enough air flow, there is no need to enable the Thermal Management function. However, sometimes the system environment is not optimized for a Celeron M or Pentium M processor board, and this requires thermal protection to guarantee a stable system. The Thermal Management feature allows system designers to design lower cost thermal solutions without compromising system integrity or reliability.

In this case both the internal and the external Thermal Monitor should be enabled. These two monitors protect the processor and the system against excessive temperatures. In this configuration the clocks will be switched on and off. At a 50% duty cycle, for example, the average power dissipation can drop by up to 50%. In this case, the processor performance also drops by about 50% since program execution halts when the clocks are removed.

Warning!

For Benchmarks and performance tests all Thermal Management functions should be disabled, if enabled the results will be erroneous due to the thermal power reduction.

7.1.2 Active Thermal Regulation

The thermal management concept of the CP306-V also encompasses active thermal regulation. For this processor, a specifically designed heat sink is employed to ensure the best possible basis for operational stability and long term reliability. Coupled together with system chassis which provide variable configurations for forced air flow, controlled active thermal energy dissipation is guaranteed.

7.1.2.1 Heat Sinks

The CP306-V is fitted with an optimally designed heat sink. The physical size, shape, and construction ensures the best possible thermal resistance (R_{th}) coefficients. In addition, it is specifically designed to efficiently support forced air flow concepts as found in a modern CompactPCI system chassis.

Even though the CP306-V is fitted with an optimally designed heat sink, the thermal energy dissipated by the high-performance Celeron M and Pentium M exceeds the thermal capabilities of the heat sink except for very low performance applications which still require the outstanding features offered by this processor. For higher performance applications, the CP306-V must be operated with forced air flow.

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7.1.2.2 Forced Air Flow

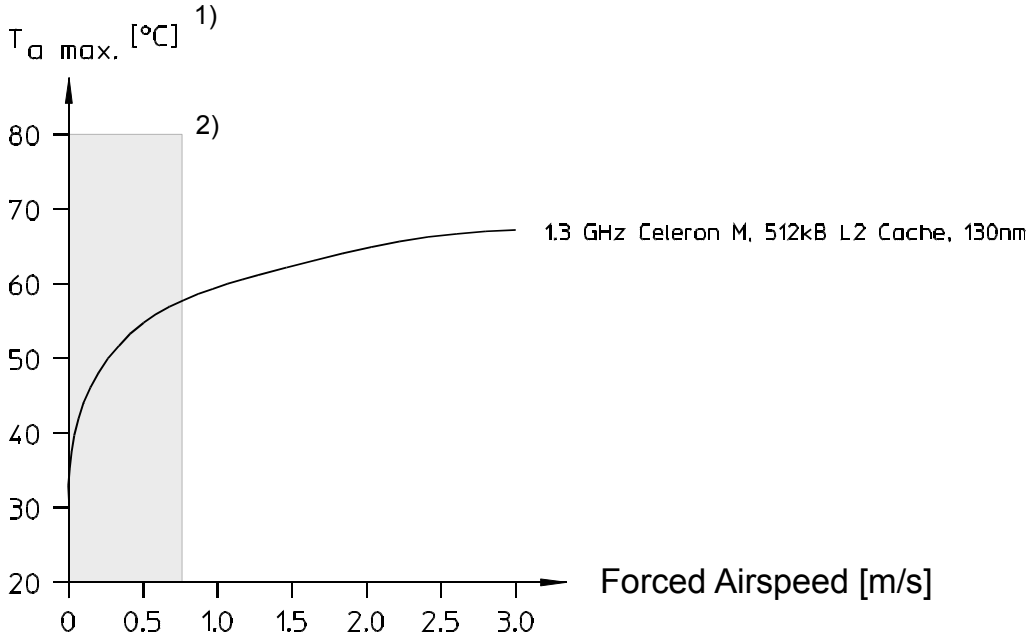
When developing applications using the CP306-V, the system integrator must be aware of the overall system thermal requirements. System chassis must be provided which satisfy these requirements. As an aid to the system integrator, a processor characteristics graph is provided for Celeron M and Pentium M processors.

The values have been measured using typical applications running under Windows 2000. In worst case situations, the values vary and the temperature range must be reduced. In all situations the maximum case temperature of Celeron M and Pentium M processors must be kept below the maximum allowable temperature. This temperature value can be measured with the onboard remote temperature sensor. To ensure functionality at the maximum temperature, the BIOS supports a temperature control feature. In instances of overtemperature the hardware monitor will reduce the processor clock speed to reduce power consumption.

The maximum case temperatures for both processor types is a follows:

- Celeron M: all versions: 100 °C
- Pentium M: all versions: 100 °C

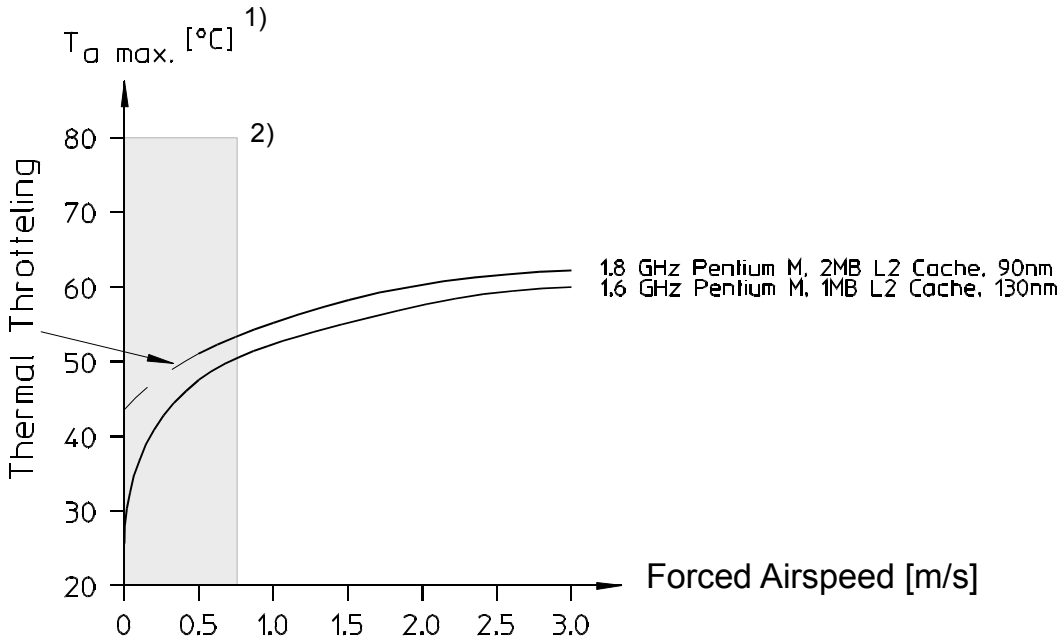
Figure 7-1: Mobile Celeron M Temperature Vs. Airspeed Graph



Warning!

1) T_a is the initial temperature of the ambient air used for convectional cooling of the board. In a typical installation where the board is mounted vertically in a system rack, this would be the temperature of the air measured at the bottom of the board before the air flows over the board.
2) If the board is to be operated within the shaded area indicated above, it is imperative to verify that it can be safely operated before the board is integrated in an application system. This will require an empirical thermal design analysis and verification by the system designer.

Figure 7-2: Mobile Pentium M Temperature Vs. Airspeed Graph



Warning!

1) T_a is the initial temperature of the ambient air used for convectional cooling of the board. In a typical installation where the board is mounted vertically in a system rack, this would be the temperature of the air measured at the bottom of the board before the air flows over the board.

2) If the board is to be operated within the shaded area indicated above, it is imperative to verify that it can be safely operated before the board is integrated in an application system. This will require an empirical thermal design analysis and verification by the system designer.

As individual processor characteristics vary as well as the system environment of the CP306-V, the information contained in Figures 7-1 must be viewed as a guide and not as an absolute specification. It is the responsibility of the system integrator to ensure that system requirements are specified accordingly.

An airflow of 1.0 m/s is a typical value for a standard *Kontron* ASM rack (3U CompactPCI rack with a 1U cooling fan tray). Newer ASMs from *Kontron* will have an airspeed of 2.0 m/s or more. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor junction temperature must never exceed the specified limit for the involved processor type.

7.1.2.3 Peripherals

When determining the themal requirements for a given application, peripherals to be used with the CP306-V must also be considered. Devices such as hard disks, CF modules, etc. which are directly attached to the CP306-V must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP306-V or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP306-V complies with the thermal considerations set forth in this document.

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Appendix A

CP306-V-IOIDE

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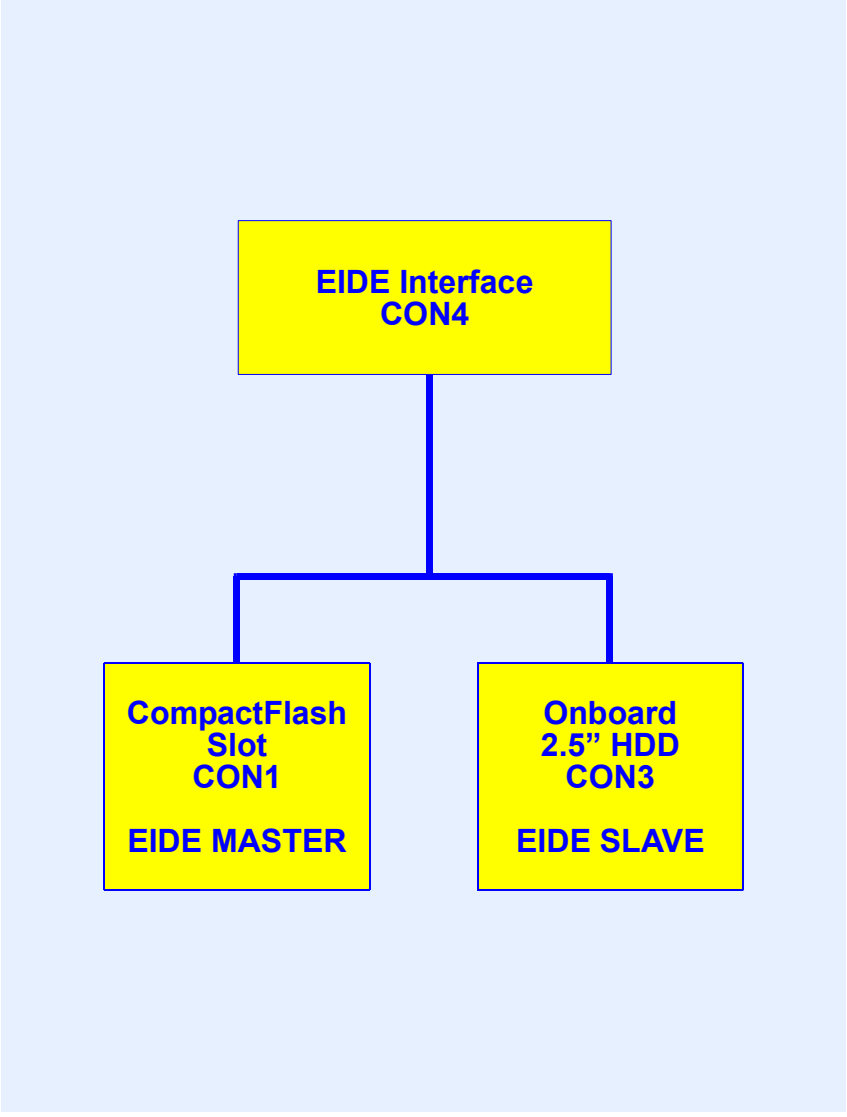
A. CP306-V-IOIDE

A.1 Overview

The CP306-V-IOIDE module has been designed to provide the CP306-V with a CompactFlash socket and an interface to a 2.5” HDD which enable the user to connect P-ATA devices to the board. Furthermore, the module provides a Reset button and an LED indicating the operation of EIDE devices. The module is connected to the 44-pin EIDE Connector J11 on the 8HP version of the CP306-V.

A.2 CP306-V-IOIDE Module Functional Block Diagram

Figure A-1: CP306-V-IOIDE Module Functional Block Diagram



A.3 CP306-V-IOIDE Module Layout

Figure A-2: CP306-V-IOIDE Module Layout - Top View

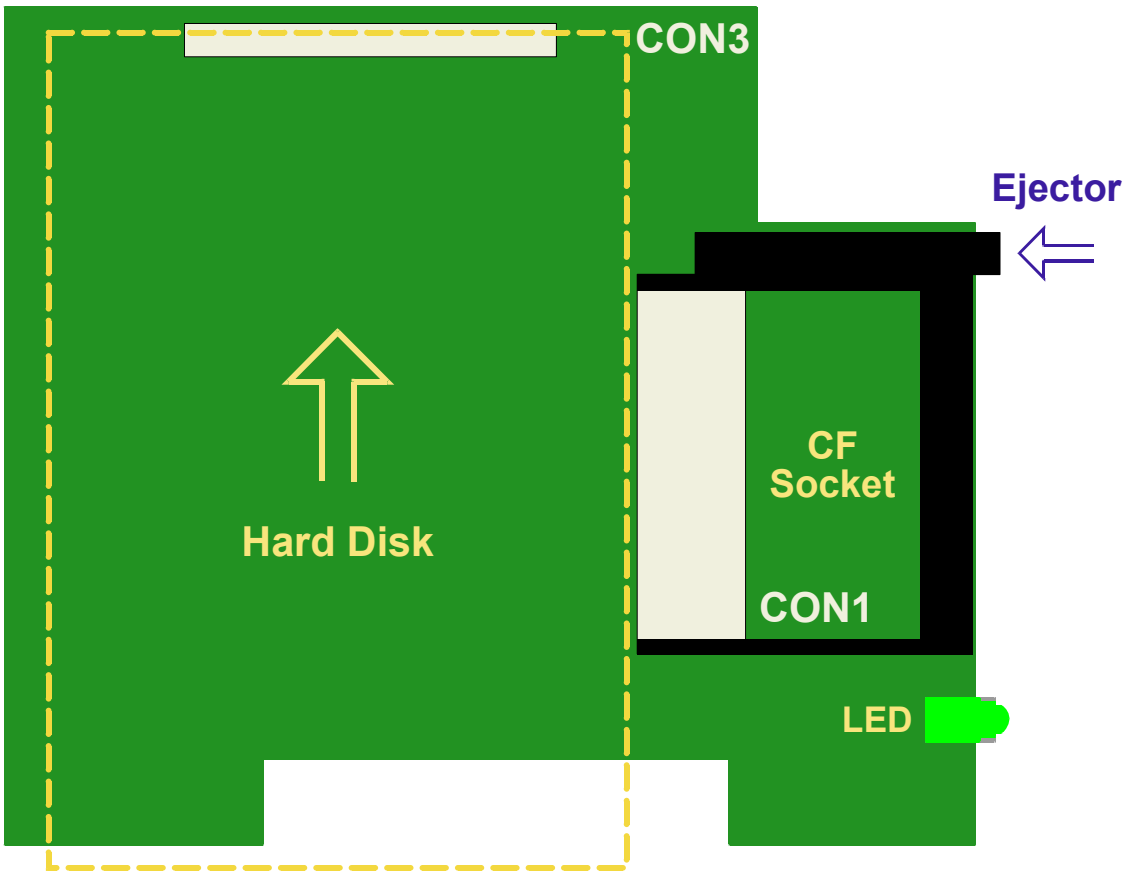


Figure A-3: CP306-V-IOIDE Module Layout - Side View

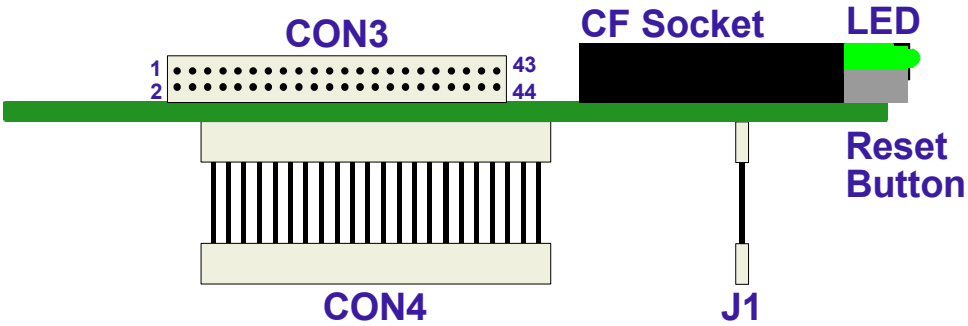


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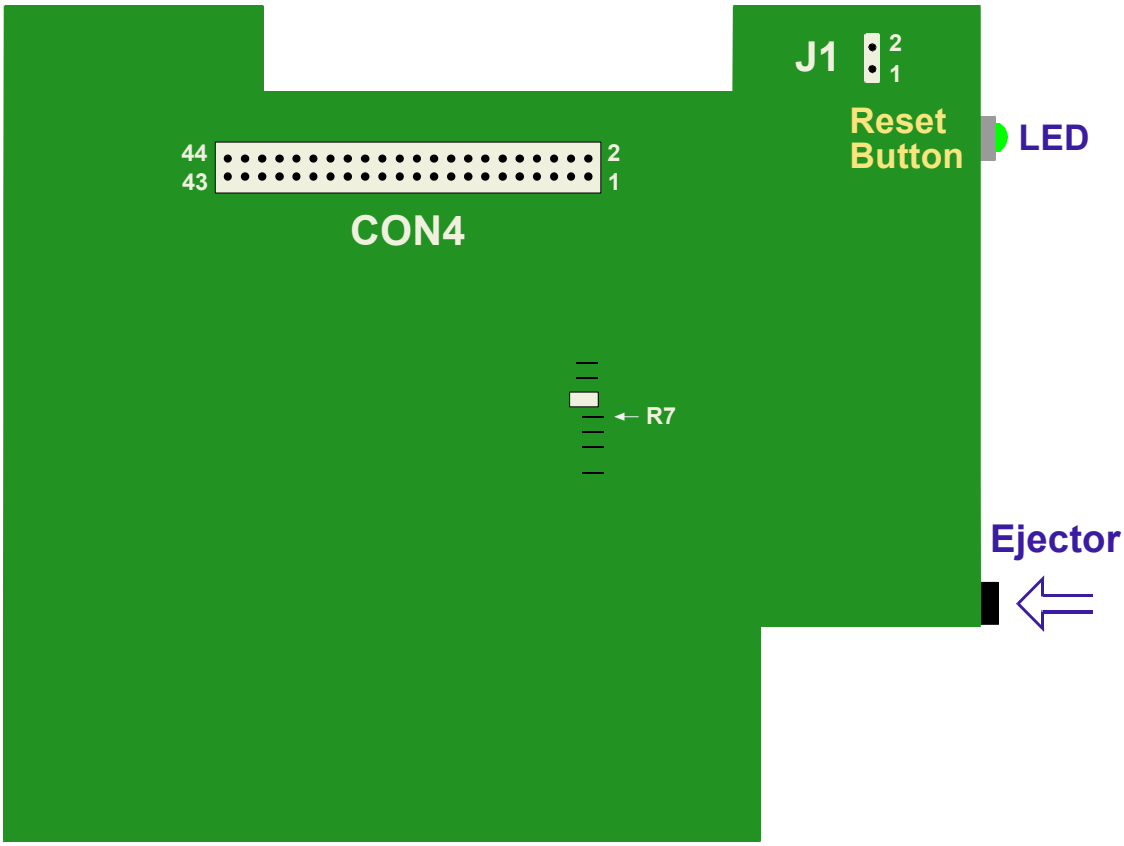
Figure A-4: CP306-V-IOIDE Module Layout - Bottom View



A.4 Module Interfaces

A.4.1 Board-to-Board Connector (Primary EIDE Port) CON4

The 44-pin, 2mm pinrow board-to-board connector CON4 is situated on the reverse of the CP306-V-IOIDE module and is used to connect the EIDE devices on the CP306-V-IOIDE module to the CP306-V baseboard.

The following table indicates the pinout of the board-to-board connector CON4.

Table A-1: Board-to-Board Connector CON4 Pinout

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	N/C	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	N/C	--	--
O	Address 1	A1	33	34	ATA66	Detect ATA66	I
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	LED driving	LED	39	40	GND	Ground signal	--
--	5V power	VCC	41	42	VCC	5V power	--
--	Ground signal	GND	43	44	N/C	--	--

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A.4.2 2.5” Hard Disk Connector CON3

A 2.5” hard disk or Flash disk may be mounted directly onto the CP306-V-IOIDE module using the 44-pin, 2mm pinrow connector CON3 situated on the front of the board.

Table A-2: Pinout of the CON3 Connector

IN/OUT	DESCRIPTION	SIGNAL	PIN	PIN	SIGNAL	DESCRIPTION	IN/OUT
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	NC	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	CSEL	Cable select	I
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	NC	--	--
O	Address 1	A1	33	34	ATA66	Detect ATA66	In
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	LED driving	LED	39	40	GND	Ground signal	--
--	5V power	VCC	41	42	VCC	5V power	--
--	Ground signal	GND	43	44	NC	--	--

Note ...

The onboard 2.5” hard disk or Flash disk connector (CON3) must be configured as a SLAVE device if a CompactFlash card is present.

A.4.3 CompactFlash Socket CON1

To enable flexible flash extension a CompactFlash (CF) type II socket is available.

CF is a very small removable mass storage device. It provides true IDE functionality compatible with the 16-bit ATA/ATAPI-4 interface and full DMA support. CF cards are also available for data storage using the Microdrive hard disk .

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The module supports both CF types (type I and type II). CompactFlash is available in both CF type I and CF type II cards. The Microdrive is a CF type II card. The CompactFlash card can be removed by pushing the ejector on the CompactFlash socket.

Warning!

The CP306-V does not support removal and reinsertion of the CompactFlash storage card while the board is in a powered-up state. Connecting or disconnecting the CompactFlash card while the power is on, which is known as "hot plugging", will result in irreparable damage to the system.

The following table provides the pinout of the CompactFlash Connector CON1.

Table A-3: CompactFlash Connector CON1 Pinout

I/O	DESCRIPTION	SIGNAL	PIN	PIN	SIGNAL	DESCRIPTION	I/O
--	Ground signal	GND	1	2	D03	Data 3	I/O
I/O	Data 4	D04	3	4	D05	Data 5	I/O
I/O	Data 6	D06	5	6	D07	Data 7	I/O
O	Chip select 0	IDE_CS0	7	8	GND (A10)	--	--
--	--	GND (ATASEL)	9	10	GND (A09)	--	--
--	--	GND (A08)	11	12	GND (A07)	--	--
--	5 V power	5 V	13	14	GND (A06)	--	--
--	--	GND (A05)	15	16	GND (A04)	--	--
--	--	GND (A03)	17	18	A02	Address 2	O
O	Address 1	A01	19	20	A00	Address 0	O
I/O	Data 0	D00	21	22	D01	Data 1	I/O
I/O	Data 2	D02	23	24	NC (IOCS16)	--	--
--	--	NC (CD2)	25	26	NC (CD1)	--	--
I/O	Data 11	D11	27	28	D12	Data 12	I/O
I/O	Data 13	D13	29	30	D14	Data 14	I/O
I/O	Data 15	D15	31	32	IDE_CS1	Chip select 1	O
--	--	NC (VS1)	33	34	DIOR	I/O read	O
O	I/O write	DIOW	35	36	5 V (WE)	5 V power	--
I	Interrupt	INTRQ	37	38	5 V	5 V power	--
O	Master/Slave	CSEL (GND pull-up)	39	40	NC (VS2)	--	--
O	Reset	Reset	41	42	IORDY	I/O ready	I
O	DMA request	DMARQ (INPACK)	43	44	DMACK	DMA acknowledge	I
I/O	Activity	DASP LED	45	46	PDIAG	ATA detection	I/O
I/O	Data 08	D08	47	48	D09	Data 09	I/O
I/O	Data 10	D10	49	50	GND	--	--

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A.4.4 Female Pinrow Connector J1

The female pinrow connector J1 is connected to the Reset connector J9 on the CP306-V baseboard. The following table indicates the pinout of the female pinrow connector J1.

Table A-4: Pinout of the J1 Connector

PIN	SIGNAL	DESCRIPTION	IN/OUT
1	RST	Reset	I
2	GND	Ground	--

A.5 Master/Slave Configuration

The hard disk and CompactFlash can be configured to master or slave. To configure the hard disk, use the jumper on the hard disk. To configure the CompactFlash, the R7 (0 ohm) resistor is used.

The following table indicates the CompactFlash Configuration.

Table A-5: CompactFlash Configuration

R7	COMPACTFLASH
open	slave
closed	***master***

The default setting is indicated by using italic bold.

A.6 Technical Specifications

Table A-6: CP306-V-IOIDE Module Main Specifications

	CP306-V-IOIDE	SPECIFICATIONS
External Interface	CompactFlash Socket	CompactFlash socket type II (true IDE mode), DMA capable
Internal Interfaces	EIDE Interface	One EIDE interface supporting Ultra ATA/100/66/33 for hard disk on 44-pin 2 mm onboard connector
General	Power Consumption	5.0 V: less than 1 mW (without CompactFlash card and hard disk)
	Temperature Range	Operating temp.: 0°C to +60°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 116 mm
	Module Weight	55 grams (without hard disk and CompactFlash card)

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Appendix B

CP-RIO3-03 Rear I/O

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B. CP-RIO3-03 Rear I/O

B.1 Overview

The CP306-V provides optional rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CPU board with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support on the system slot.

The CP-RIO3-03 Rear I/O provides the following interfaces.

- Two USB ports (USB 2.0)
- One Fast Ethernet port without LED
- Two COM ports
- VGA CRT interface
- Primary EIDE port
- Fan control input
- PS/2 for mouse and keyboard

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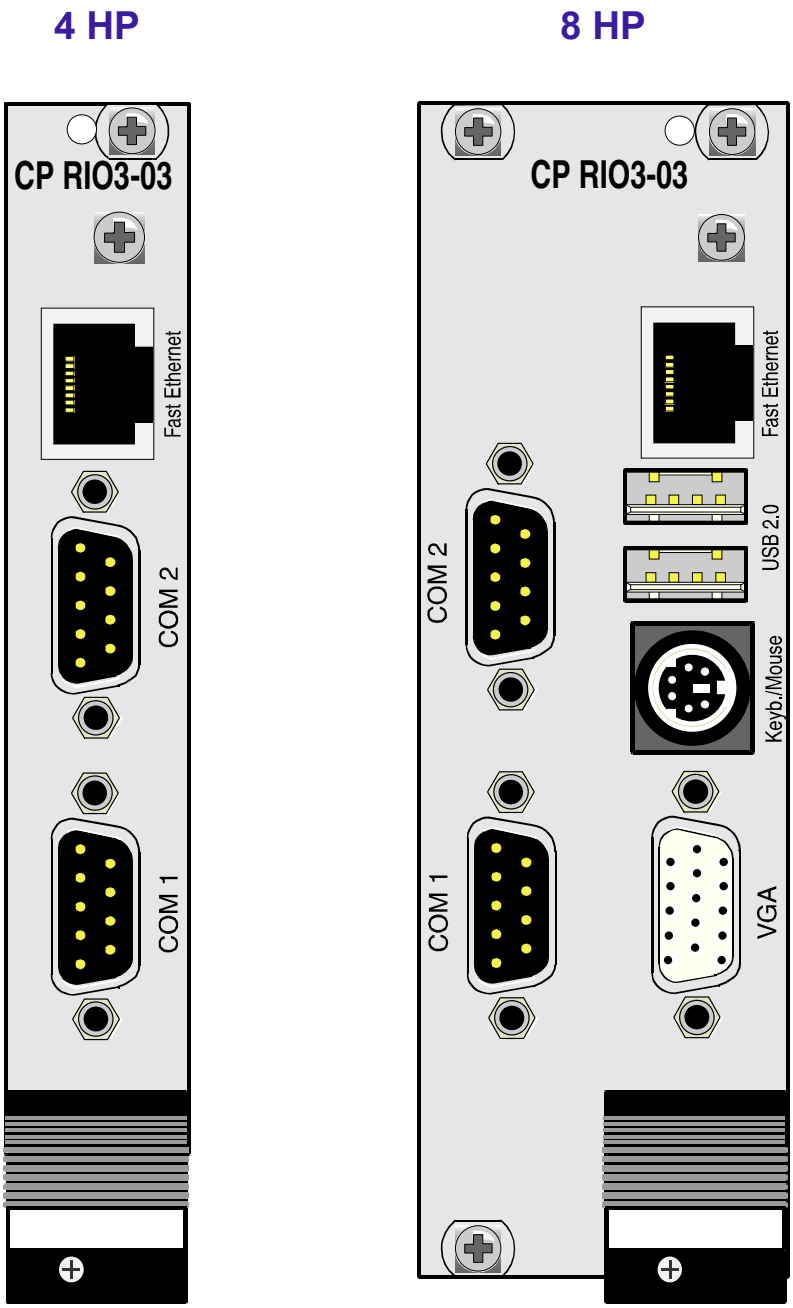
B.2 Front Panels

Figure B-1: CP-RIO3-03 Rear I/O Front Panels, 4HP and 8HP Versions



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B.3 Module Layout: 4HP and 8HP Versions

Figure B-2: CP-RIO3-03 Rear I/O Module Layout, 4HP Version

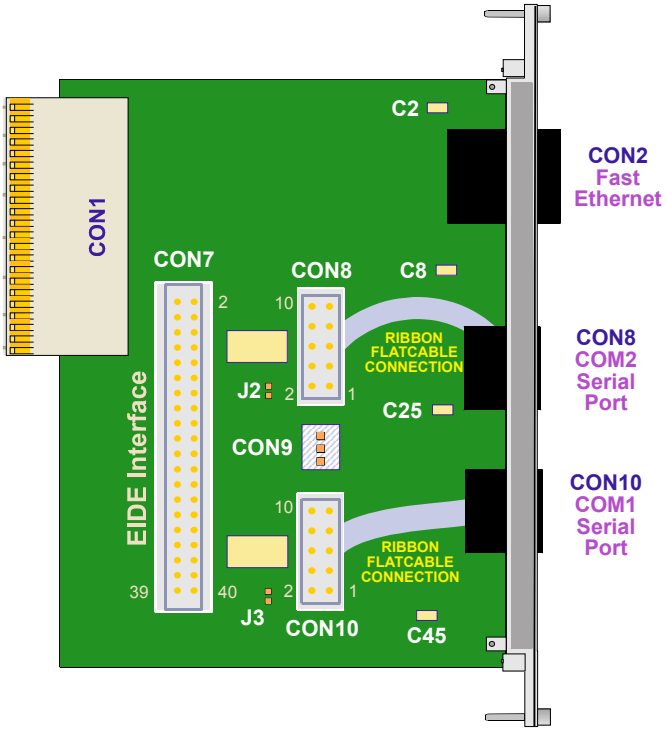
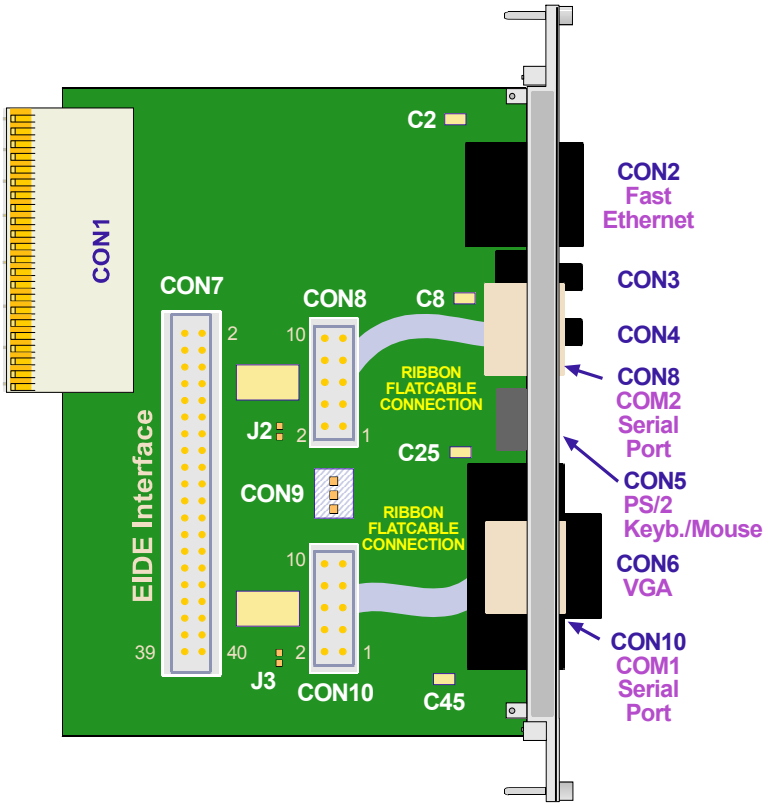


Figure B-3: CP-RIO3-03 Rear I/O Module Layout, 8HP Version



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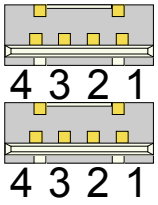
B.4 Module Interfaces

B.4.1 USB Interfaces

There are two identical USB interfaces on the CP-RIO3-03 Rear I/O module (8HP version) each with a maximum transfer rate of 480 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

Figure B-4: USB Connector CON3/CON4



The following table indicates the pinout of the USB connectors CON3/CON4.

Table B-1: USB Connector CON3/CON4 Pinout

PIN	SIGNAL	DESCRIPTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--

Note ...

The USB power supply to the USB connector provides 500 mA continuous load current a short-circuit protection (900 mA). All the signal lines are EMI filtered.

Note ...

The rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 metres.

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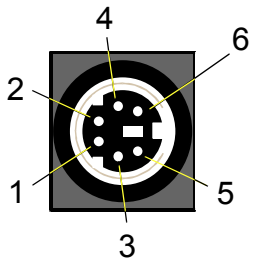
B.4.2 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

Figure B-5: Keyboard/Mouse Connector CON5



The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded Mini-DIN connector. The keyboard and mouse power supply (VCC) provides 500 mA continuous load current and a short-circuit protection (900 mA). All the signal lines are EMI filtered.

Table B-2: Keyboard/Mouse Connector CON5 Pinout

PIN	SIGNAL	DESCRIPTION	IN/OUT
1	KDATA	Keyboard data	I/O
2	MDATA	Mouse data	I/O
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	O
6	MCLK	Mouse clock	O

Note ...

The keyboard and mouse power supply (VCC) provides 500 mA continuous load current and a short-circuit protection (900 mA). All the signal lines are EMI filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector is available from *Kontron.*

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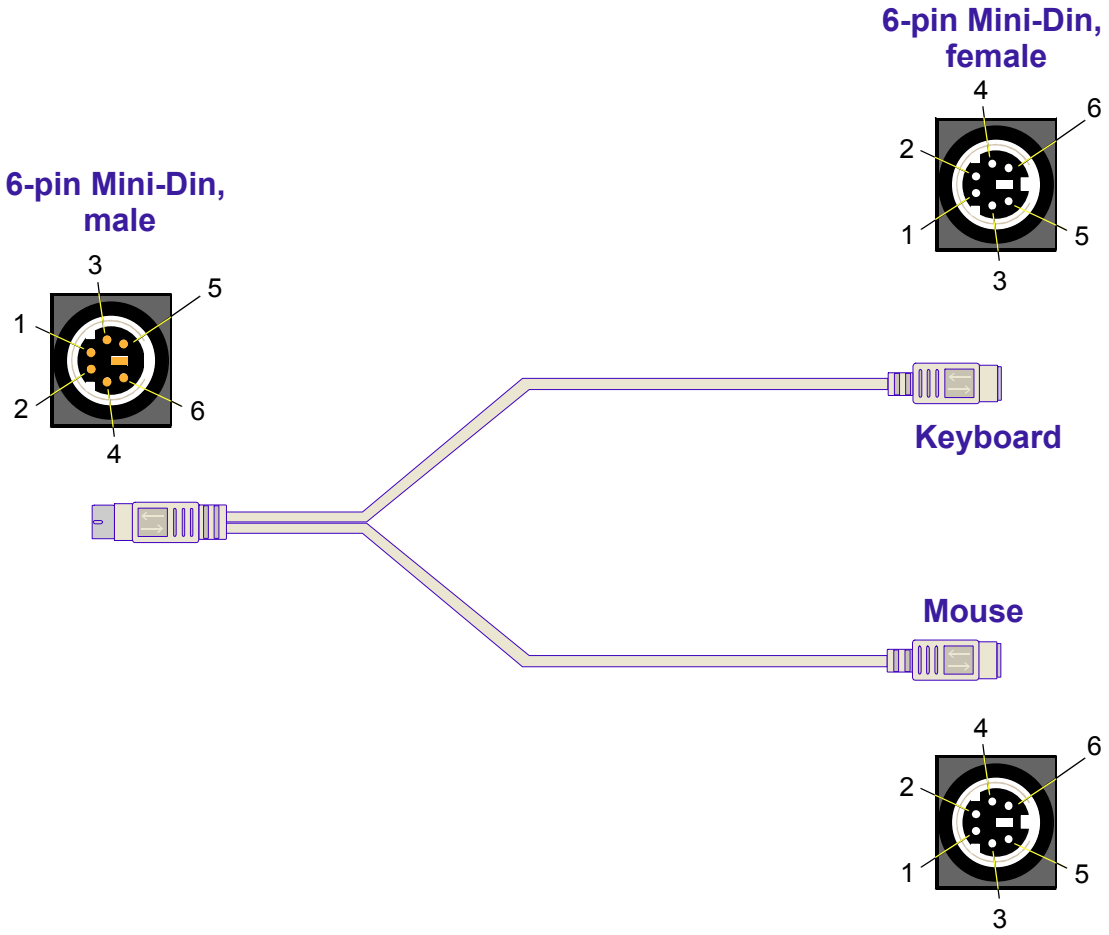
Figure B-6: Adapter for Connecting Mouse/Keyboard via PS/2



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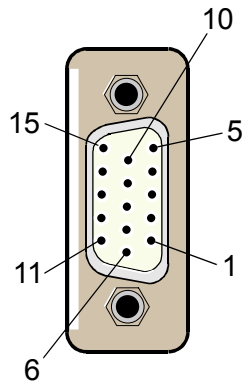
B.4.3 VGA Interface

The 15-pin female connector CON6 is used to connect a VGA monitor to the CP-RIO3-03 Rear I/O (8HP version) board.

Figure B-7: D-SUB VGA Connector



The following table indicates the pinout of the VGA Connector CON6.

Table B-3: VGA Connector CON6 Pinout

D-SUB 15	SIGNAL	DESCRIPTION	IN/OUT
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	Not supported	I/O
15	Sclk	Not supported	O
9	VCC	Power +5V 200 mA no fuse protection	O
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

Note ...

The 75 ohm termination resistors for the three VGA signals (red, green, blue) are located on the baseboard.

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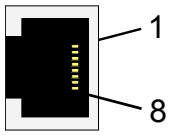
B.4.4 Fast Ethernet Interface

The Ethernet connector is realized as an RJ45 twisted-pair connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.

Figure B-8: Ethernet/Fast Ethernet Connector



CON2 supplies the 10Base-TX/100Base-TX interface to the Ethernet controller.

The following table indicates the pinout of the RJ45 Connector CON2.

Table B-4: RJ45 Connector CON2 Pinout

RJ45	SIGNAL	DESCRIPTION
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

Note ...

The maximum length of cabling over which the Ethernet transmission can operate effectively depends upon the transceiver in use.

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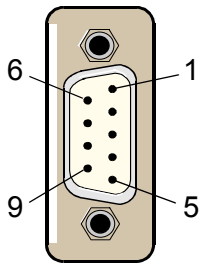
B.4.5 Serial Port Interfaces

Figure B-9: PC-Compatible D-SUB Serial Interface



The serial port male connectors CON8 and CON10 allow the connection of RS232 devices to the CP-RIO3-03 Rear I/O board and have the following pinout.

Table B-5: Serial Port Connectors CON8 and CON10 Pinouts

D-SUB 9	SIGNAL	DESCRIPTION	IN/OUT
1	DCD	Data carrier detect	I
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	GND	Signal ground	--
6	DSR	Data send request	I
7	RTS	Request to send	O
8	CTS	Clear to send	I
9	RI	Ring indicator	I

B.4.6 Fan Control Interface (Optional)

A fan for CPU cooling can be connected via the power connector CON9.

Table B-6: Fan Control Connector CON9 Pinout

PIN	DESCRIPTION
1	Ground
2	5V Fan Supply Voltage at a maximum current of 300 mA
3	Fansense

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B.4.7 EIDE Interface

The EIDE interface and the CP306-V onboard CompactFlash socket share the same signals and are connected to the primary EIDE port.

Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable also supports all legacy IDE drives.

Due to the rear I/O configuration it is strongly recommended to use only a very short cable length. The maximum cable length should not exceed 45 cm.

The blue end of the ATA-100 cable must be connected to the motherboard, the gray connector to the UltraDMA/100 slave device and the black connector to the UltraDMA/100 master device.

The following table sets out the pinning of connector CON7 and details its corresponding signal names and functions.

Table B-7: Pinout of AT Standard EIDE Connector CON7

IN/OUT	DESCRIPTION	SIGNAL	PIN	PIN	SIGNAL	DESCRIPTION	IN/OUT
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	NC	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	ATA100	Detect ATA100	--
O	Address 1	A1	33	34	NC	--	--
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
--	--	NC	39	40	GND	Ground signal	--

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B.4.8 Rear I/O interface on Compact PCI Connector CON1

The CP-RIO3-03 Rear I/O conducts a wide range of I/O signals through the fear I/O connector CON1.

Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. Failure to comply with the above may result in damage to your board.

Table B-8: Rear I/O CompactPCI Bus Connector CON1 Pinout

PIN	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	KDAT	UV2-	UV4+	RTC Bat	+3.3V	GND
17	GND	KCLK	ROUT (GND)	PRST#	REQ6#	GNT6#	GND
16	GND	PMDAT	UV2+	DEG#	GND	UV4-	GND
15	GND	PMCLK	GOUT (GND)	FAL#	REQ5#	GNT5#	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE1 (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	IDE_PD[9]	1DCD	1RIN	GND
10	GND	IDE_PD[8]	IDE_RST#	1TXD	IDE_PD[10]	1RXD	GND
9	GND	IDE_PD[6]	IDE_PD[7]	IDE_PD[4]	IDE_PD[5]	IDE_PD[11]	GND
8	GND	IDE_PD[3]	IDE_PD[12]	IDE_PD[2]	GND	IDE_PD[1]	GND
7	GND	IDE_PD[14]	IDE_PD[0]	IDE_PD[15]	IDE_PDRQ#	IDE_PIOW#	GND
6	GND	IDE_PIOR	IDE_PIORDY	IDE_PDACK#	IDE_PD [13]	IDE_PIRQ14	GND
5	GND	IDE_PA[1]	GND	IDE_PA[0]	IDE_PA[2]	TH_GP/SLP_S3	GND
4	GND	VIO	VCC	IDE_PCS1#	GND	IDE_PCS3#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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Legend for table on preceding page

IDE Signals

IDE	Primary IDE signals

Ethernet1

TDP1/TDN1	Transmit Differential Pair.
RDP1/RDN1	Receive Differential Pair.

USB ports

USB1+/-	USB data differential data signals
USB3+/-	USB data differential data signals

Serial Ports 1 and 2

S1	COM1 Serial port signals; TTL level
S2	COM2 Serial port signals; TTL level

PS/2 Ports

KDAT/KCLK	PS/2 Keyboard signals
PMDAT/PMCLK	PS/2 Mouse signals

CONTROL Signals

FANSENSE	Schmitt Trigger fan tachometer inputs; TTL level
TH_GP/SLEP_S3	General purpose output, TTL level This signal indicates the sleep state of S3.

VGA CRT signals

ROUT	Red signal
GOUT	Green signal
BOUT*	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.

* Note that this signal (BOUT) appears twice in the rear I/O CompactPCI bus connector J2 pinout in order to provide compatibility with the CP302. Pin number B11 refers to the CP306-V and C13 refers to the CP302. The default configuration is CP306-V (B11).

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Reserved Signals

RES	Reserved (leave open)

B.5 Jumper Setting

B.5.1 COM Port Configuration

The two COM ports are configured using solder jumpers J2 and J3

B.5.1.1 COM1 Configuration

Table B-9: COM1 Configuration using Jumper J3

J3	FUNCTION
Open	***RS232 enabled***
Closed	RS232 disabled

The default setting is indicated by using italic bold.

B.5.1.2 COM2 Configuration

Table B-10: COM2 Configuration using Jumper J2

J2	FUNCTION
Open	***RS232 enabled***
Closed	RS232 disabled

The default setting is indicated by using italic bold.

B.5.2 Shorting Chassis GND (Shield) to Logic GND

The front panel including the front panel connectors are isolated to the logic ground. This zero Ohm resistor enables connection between the chassis GND and logic GND.

Table B-11: Shorting Chassis GND (Shield) to Logic GND

C2, C8, C25, C45	FUNCTION
Open	***Connectors are isolated to logic GND***
Short	Connectors are connected to logic GND and chassis GND

The default setting is indicated by using italic bold.

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